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Novel high functionality fault tolerant ALU

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ABSTRACT

Miniaturization, cost, functionality, complexity and power dissipation are important and necessary design traits which need attention in circuit designing. There is a trade off between miniaturization and power dissipation. Smart technology is always searching for new paradigms to continue improve power dissipation. Reversible logic is one of smart computing deployed to avoid power dissipation. Researchers have proposed many reversible logic-based arithmetic and logic units (ALU). However, the research in the area of fault tolerant ALU is still under progress. The aim of this paper is to bridge the knowledge gap for a new researcher in area of fault tolerance using parity preserving logic gates rather than searching huge data through various sources. This paper also presents a high functionality based novel fault tolerant arithmetic and logic unit architecture. A comparison on optimization aspects is presented in tabular form and results shows that proposed ALU architecture is optimum balance in terms of all aspects of reversible logic synthesis. The proposed ALU architecture is coded in Verilog HDL and simulated using Xilinx ISE design suit 14.2 tool. The quantum cost of all gates used in proposed architecture is verified using RCViewer + tool.

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1. INTRODUCTION

Reversible computing is found to be one of the emerging and promising technologies to overcome power dissipation due to loss of bits. Rolf Landauer [1] and C.H. Bennett [2], jointly addressed the issue and shown the direction to work in this area. A significant work has been already done by many researchers and efficient architectures have been investigated. Smart reversible computing is incorporating fault tolerance mechanism in existing architectures. Circuit designed for any application is reliable and robust only if fault coverage and testable features are embedded into it. Fault tolerance embedding avoids additional hardware and complexity overhead. In order to achieve robustness and making reversible logic based designed system fault tolerant; parity preserving logic gates are used. Complex computing environment is switching from peta scale to exa scale and fault tolerant ALU is heart of it.

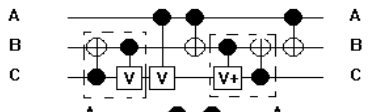
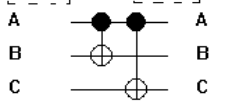
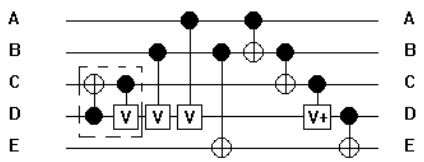
Parity preserving logic gates are based on principle of holding parity. If input vector (ABC) of 3*3 gate holds even/odd parity, then output vector (PQR) should also hold even/odd parity. Conservative gate is not only parity preserving but it also maintains equal number of 1's in both input and output vectors. It is easy to investigate parity preserving reversible logic gate but making it conservative is a bit intractable.

Fredkin gate is exclusively designed to maintain conservative property. Researchers have investigated many parity preserving logic gates. Some of them are one through and conservative also. Most of the researches have shown quantum equivalence of their proposed gates and defined their corresponding quantum cost yet quantum cost of some is still unknown and need to be investigated like PRUG and PPPG gates.

In the past few years researchers have made efforts to design reversible logic based ALU [3-6]. However, till now available research results on fault tolerant arithmetic logic unit are very few. Guan et al. [6] proposed optimized arithmetic and logic circuit but fault tolerance is missing in their design. Rakshith and Saligram [7] proposed fault tolerant arithmetic logic unit using parity preserving logic but complexity of circuit is high for n bit ALU as divide and conquer approach is missing. Many other researchers have obtained good results in ALU optimization [8, 9]. Saligram et al., [10] have proposed two faults tolerant ALU architectures but quantum cost of both circuits is unspecified. Bashiri and Haghparast [11] proposed fault tolerant ALU architecture but garbage and ancillary lines remain unoptimized as compare to number of operations performed. Authors proposed and analyzed a basic model of fault tolerant reversible ALU but quantum cost is high and number of operations are limited [12]. Fault tolerance is incorporated in 1-bit ALU structure based on 7 parity preserving gates including FTRA, Fredkin and double Feynman gates. There is optimum utilization of resources but functionality is limited [13]. Moallem et al., [14] provided another approach of designing arithmetic and logic unit but fault tolerance feature is not added to circuit. Another unique approach of ALU design is presented in research work [15]. Sen et al., [16] proposed 1-bit ALU structure but many design traits remain unoptimized. Proposed design does not even support fault tolerance.

Thakral and Bansal [17] proposed fault tolerant ALU architecture using parity preserving logic gates but unable to prove it completely fault tolerant due to use of HNG gate. Some researchers have investigated parity preserving reversible logic-based gates and utilized them to design fault tolerant ALU but quantum cost of their proposed ALU remains unspecified [18, 19]. Implementation and comparative analysis of existing ALU designs is focussed to investigate scope of improvement in state of the art [20]. In 2016, Misra et al., [21] proposed new technique for fault tolerant ALU design with 32 operations but there are some redundant operations. Rahimpour and Jafari [22] proposed fault tolerant ALU using QCA technology QCA analysis shows good results as far as delay and area are concerned but functionality and quantum cost also need to be focused in this work. Bahadori et al., [23] proposed reversible control unit with fault tolerance mechanism. The quantum cost is optimum in terms of number of operations but for complete ALU, quantum cost will rise with circuit expansion. Das and Chandaran [24] proposed 1-bit ALU incorporated with fault tolerance. There is optimum utilization of resources like constant input lines, garbage output lines and gate count as far as number of operations are concerned but there is scope of improvement of its functions and quantum cost. Thakral and Bansal [25, 26] proposed reduced quantum cost-based fault tolerant ALU architectures. Each existing design has some advantages and limitations. However, there is a lot of scope for further improvement of optimization metrics like quantum cost, ancillary inputs, number of operations and garbage outputs. This paper presents a novel low complex and high functionality-based fault tolerant arithmetic logic unit. Proposed fault tolerant arithmetic logic unit is designed based on conservative and parity preserving "Fredkin", low quantum cost parity preserving based "Double Feynman" and high functionality parity preserving based "FTRA" gates. A brief insight into used parity preserving logic gates along with expression and quantum implementation is given in Table 1. The methodology of proposed ALU design, proposed novel architecture, design traits comparison and conclusion are given in section 2 to 5.

Table 1. Popular parity preserving logic gates

Reversible logic gate	Expression	Quantum implementation
Fredkin	$P = A$ $Q = \overline{A}\ B \oplus AC$ $R = \overline{A}\ C \oplus AB$	
Double Feynman	$P = A$ $Q = A \oplus B$ $R = A \oplus C$	
Fault tolerant reversible adder (FTRA)	$P = A$ $Q = B$ $R = A \oplus B \oplus C \oplus D$ $S = (A \oplus B)(C \oplus D)$ $\oplus(\overline{A}\ B \oplus D) \oplus E$	

2. METHODOLOGY OF PROPOSED DESIGN

The proposed fault tolerant arithmetic logic unit architecture is designed to keep in view enhancing functionality. Proposed circuit is designed using six "Fredkin" gates, four "Double Feynman" gates and one "FTRA gate" which are parity preserving gates. Proposed Circuit is shown in Figure 1. "Double Feynman gate 1" is passing B or B' as per select line S0. "Fredkin gate 1" is acting as 2:1 multiplexer. S2 and T1 are inputs of multiplexer and S1 is acting as selection line. "Fredkin gate 1" is passing 0, 1, B and B' as per desired logic depending upon combination of S1 and S2. "Double Feynman gate 2" is duplicating as well as inverting the input signal. "Double Feynman gate 2" is passing B or B' as per desired logic depending upon select line S3. "Fredkin gate 2" is acting as 2:1 multiplexer. S5 and T3 are two input lines and S3 is acting as select line. It is passing S5 (logic 0 /logic 1) or T3 (signal B/B') as per desired logic depending upon combination of S4 and S5. "Double Feynman gate 3" is duplicating as well as inverting input signal as per requirement. "Double Feynman gate 3" is passing A as well as A' as per desired logic depending upon select lines S6 and S7. "Double Feynman gate 4" is used to avoid fan out problem and copying S8 signal on all three output lines. "Double Feynman gate 4" is passing '0' or '1' chosen by select line S8. "Fredkin gate 3" is passing logic '0' or logic '1' or signal A or AB or AB' or A'B or A+B or A+B' as per desired logic depending upon combination of T6, T4 and T7. If T7 is 0, then AND of complement of signal on T6 input line and signal on T4 input line is produced on T8 output line. If T7 is 1, Then OR of signals on T6 and T4 input lines is produced on T8 output line.

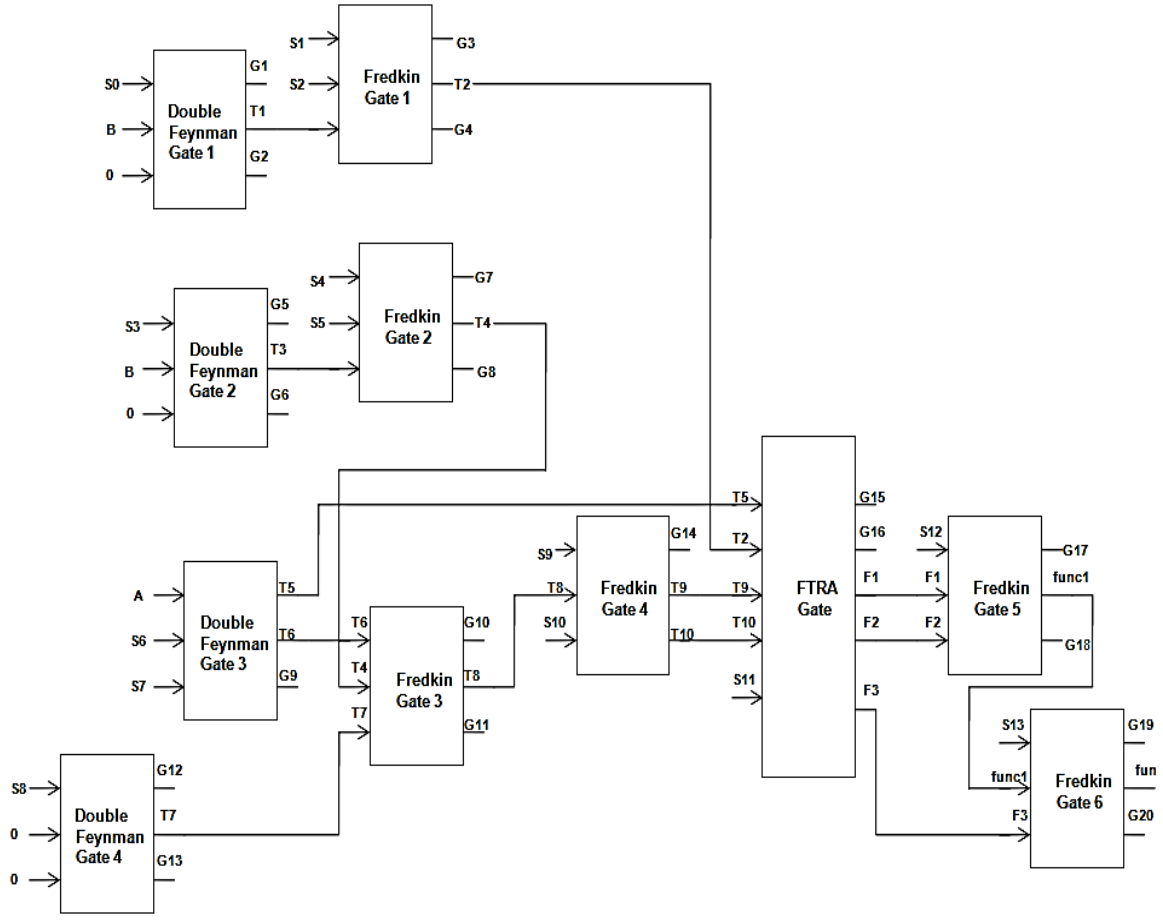


Figure 1. Proposed high functionality fault tolerant reversible ALU architecture

"FTRA gate" is 5x5 parity preserving fault tolerant reversible adder gate which can work as full adder as well as full subtractor along with performing other logical operations; proving it to be a universal logic gate. FTRA is operated under various combinations of selection lines to perform 12 logical operations and 28 arithmetic operations. In total it can perform 40 operations. This high functionality proves it to be optimum arithmetic logic unit. Fourteen selection lines are used to control operation of arithmetic and logic unit. For performing logical operations, S3 is put don't care, S4, S6 and S7 are put to zero. Logical operations

XOR, XNOR, A and A' are obtained on F1 output line, AND, NOR, OR, NAND are obtained on F2 line and (A+B'), (A'+B), AB', A'B are obtained on F3 output line. If input vector of FTRA is considered as A,B,C,D,E and output vector is considered as P,Q,R,S,T then FTRA works as full adder with three inputs A,B and Cin are provided on A,B,C lines and D, E are put to zero . In this arrangement, sum is obtained on R line and Cout is obtained on S line. While for subtraction inputs A, B and Bin are provided on A, B and D lines respectively and C, E are put to zero. In this arrangement, Difference is obtained on R line and Bout is obtained on T line. "Fredkin gate 5" is acting as 2:1 multiplexer. F1 and F2 are two input lines and S12 is acting as select line. It is passing F1 or F2 on func1 output line as per desired logic depending upon select line S12. "Fredkin gate 6" is acting as 2:1 multiplexer. It is passing func1 (F1 or F2) or F3 on func output line as per desired logic depending upon select line S13.

3. PROPOSED FAULT TOLERANT ALU ARCHITECTURE

The proposed Fault tolerant ALU architecture is configured to perform 40 operations including 12 logical and 28 arithmetic operations. List of logical operations performed by proposed arithmetic and logical unit is shown in Table 2. For performing logical operations; S3 is put to don't care condition while S4, S6, S7 and S9 are put to 0. List of arithmetic operations are divided into two sets. Arithmetic operations set 1 comprises of addition related operations and Arithmetic operations set 2 comprises of subtraction related operations. For set-1operations; S9, S10, S11, S12 and S13 are put to 0 while for set-2 operations; S9 is put equal to 1 and S10, S11, S12 and S13 are put to 0. List of arithmetic operations performed by proposed arithmetic and logic unit is shown in Table 3. Total operations count is 40 making it high functionality fault tolerant arithmetic and logical unit. Proposed high functionality fault tolerant reversible ALU architecture is shown in Figure 1. As proposed novel architecture consists of six Fredkin gates (with quantum cost of 5 each), four double Feynman gates (with quantum cost of 2 each) and one FTRA gate with quantum cost of 8. Therefore, total quantum cost calculated is 46. The simulation waveform of proposed high functionality fault tolerant reversible ALU architecture is shown in Figure 2

Table 2. Logical operations

S0	S1	S2	S5	S8	S10	S11	S12	S13	func
0	1	x	0	0	0	1	0	0	A XOR B
0	1	X	0	0	0	1	1	0	A AND B
0	1	X	0	0	0	1	X	1	A+B'
0	1	X	0	0	1	0	0	0	A XNOR B
0	1	X	0	0	1	0	1	0	A NOR B
0	1	X	0	0	1	0	X	1	A'+B
0	1	X	1	1	0	0	1	0	A OR B
0	1	X	1	1	0	0	X	1	AB'
0	1	X	1	1	1	1	1	0	A NAND B
0	1	X	1	1	1	1	X	1	A'B
X	0	0	0	0	0	1	0	0	A
X	0	1	0	0	0	1	0	0	A'

Table 3. Arithmetic operations

S0	S1	S2	S3	S4	S5	S6	S7	S8	Func (Set-1)	Func (Set-2)
X	0	0	1	1	X	1	1	0	A plus AB'	A minus AB'
1	1	X	0	1	X	1	1	0	A plus B' plus AB	A minus B' minus AB
0	1	X	1	1	X	1	1	0	A plus B plus AB'	A minus B minus AB'
0	1	X	X	0	0	0	0	0	A plus B	A minus B
1	1	X	X	0	0	0	0	0	A plus B'	A minus B'
X	0	0	0	1	X	1	1	0	A plus AB	A minus AB
1	1	X	X	0	0	0	0	1	A plus B' plus A	A minus B' minus A
0	1	X	X	0	0	0	0	1	A plus B plus A	A minus B minus A
X	0	0	0	1	X	0	0	0	A plus A'B	A minus A'B
0	1	X	0	1	X	0	0	0	A plus B plus A'B	A minus B minus A'B
1	1	X	0	1	X	0	0	0	A plus B' plus A'B	A minus B' minus A'B
X	0	0	0	1	X	0	0	1	A plus (A+B)	A minus (A+B)
X	0	0	1	1	X	0	0	1	A plus (A+B')	A minus (A+B')
X	0	0	X	0	0	0	0	1	A plus A	A minus A

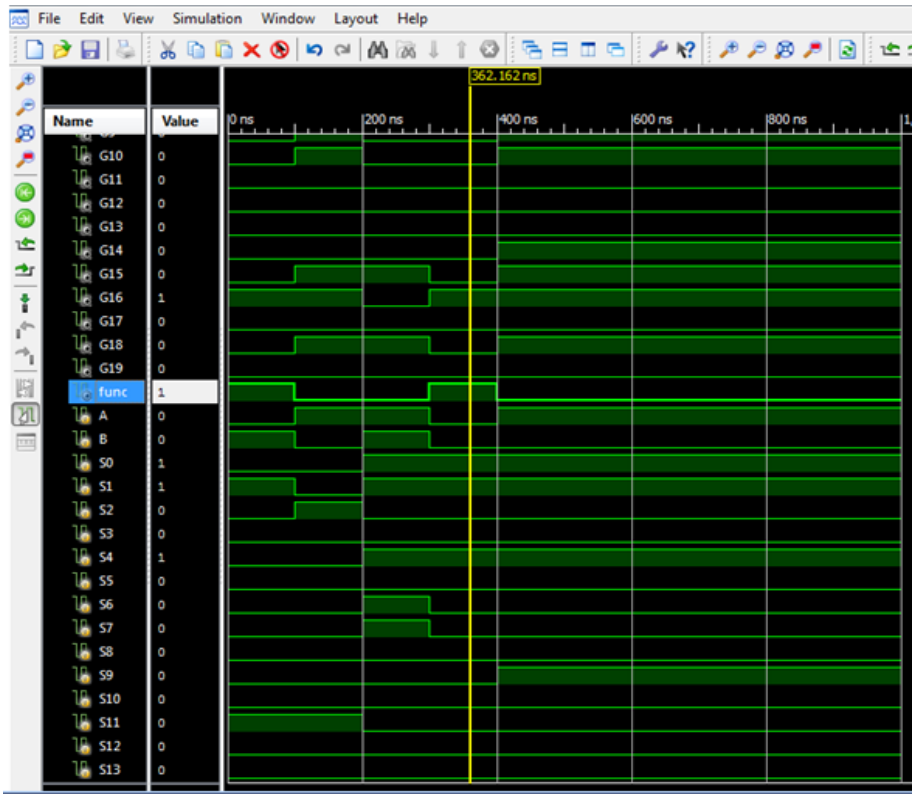


Figure 2. Simulation waveform of proposed fault tolerant reversible ALU architecture

4. COMPARISON AND RESULTS

The proposed novel high functionality fault tolerant ALU architecture is compared with Design 1 [6], Design 2 [7] and Design 3 [21] in terms of important reversible design traits. The proposed architecture is designed with minimum quantum cost; 46 and highest operations: 40. There is drastic reduction in reversible logic gates, constant input lines and complexity is also avoided. Reversible design trait comparison sheet of various ALU designs is presented in Table 4. A comparison on optimization aspects is presented in tabular form and results shows that proposed ALU architecture is optimum balance in terms of all aspects of reversible logic synthesis. Bar chart representation is shown in Figure 3 to compare evaluation results and clear understanding.

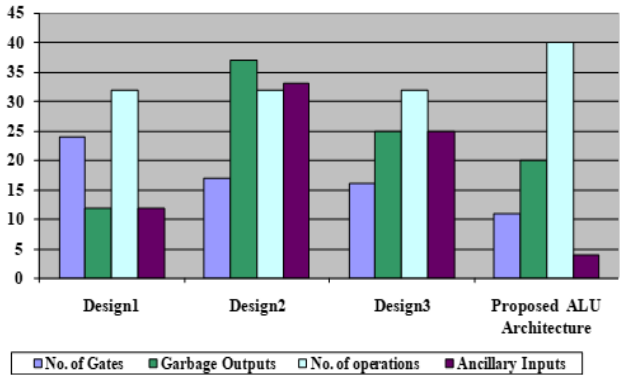


Figure 3. Bar chart comparison for quantitative analysis

Table 4. Reversible design trait comparison sheet

ALU DESIGNS	Design 1 [6]	Design 2 [7]	Design 3 [21]	Proposed Fault Tolerant ALU Architecture
No. of Gates	24	17	16	11
Quantum Cost	70	595	77	46
Operations	32	32	32	40
Garbage Outputs	12	37	25	20
Ancillary Inputs	12	33	25	4
Fault Tolerance	No	Yes	Yes	Yes

5. CONCLUSION

The proposed novel high functionality fault tolerant ALU design promises the low quantum cost and high functionality as compare to other existing designs. The bar chart comparison of proposed novel high

functionality fault tolerant ALU design over existing ALU design 1, 2 and 3 quantitatively demonstrates 25% increase in functionality with 40% reduction in quantum cost as compare to best results in literature. Fault tolerance and test patterns not only make system robust but also demanded by smart computing required for industrial and commercial applications. This research may be further extended for multibit fault detection and correction along with functionality enhancement.

REFERENCES

[1] Landauer R., "Irreversibility and Heat Generation in the Computing Process," *IBM Journal of Research and Development*, vol. 5, no. 3, pp. 183-191, 1961.

[2] Bennett C., "Logical Reversibility of Computation," *IBM Journal of Research and Development*, vol. 17, no. 6, pp. 525-532, 1973.

[3] Thomsen M., Glück R., Axelsen H., "Reversible Arithmetic Logic Unit for Quantum Arithmetic," *Journal of Physics A: Mathematical and Theoretical*, vol. 43, no. 38, 2010.

[4] Matthew M, Matthew L, Richard M, Nagarajan R., "Design of a Novel Reversible ALU using an Enhanced Carry Look Ahead Adder," *11th IEEE International Conference on Nanotechnology*, 2012.

[5] Syamala Y, Tilak A., "Reversible Arithmetic Logic Unit," *2011 3rd International Conference on Electronics Computer Technology*, 2011.

[6] Guan Z., Li W., Ding W., Hang Y., Ni L., "An Arithmetic Logic Unit Design Based on Reversible Logic Gates," *Proceedings of 2011 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing*, 2011.

[7] Rakshith, T.R. and Saligram, R., "Parity Preserving Logic Based Fault Tolerant Reversible ALU," *2013 IEEE Conference on Information & Communication Technologies*, 2013.

[8] Singh R, Upadhyay S, S S, Jagannath K, Hariprasad S., "Efficient Design of Arithmetic Logic Unit using Reversible Logic Gates," *International Journal of Advanced Research in Computer Engineering & Technology (IJARCET)*, vol. 3, no. 4, pp. 1474-1477, 2014.

[9] Gupta A, Malviya U, Kapse V., "Design of Speed, Energy and Power Efficient Reversible Logic Based Vedic ALU for Digital Processors," *2012 Nirma University International Conference on Engineering (NUiCONE)*, 2014.

[10] Saligram R., Shridhar Hegde S., A. Kulkarni S, H.R. Bhagyalakshmi, M.K. Venkatesha, "Design of Parity Preserving Logic Based Fault Tolerant Reversible Arithmetic Logic Unit," *International Journal of VLSI Design & Communication Systems*, vol. 4, pp. 53-68, 2013.

[11] Bashiri R., HaghparastM., "Designing a Novel Nanometric Parity Preserving Reversible ALU," *Journal of Basic and Applied Scientific Research*, vol. 3, no. 6, pp. 572-580, 2013.

[12] Safari P., Haghparast M., Azari A., Branch A., "A Design of Fault Tolerant Reversible Arithmetic Logic Unit," *Life Science Journal*, vol. 9, no. 3, pp. 643-646, 2012.

[13] Sen B., Ganeriwal S., Sikdar B. K., "Reversible Logic-Based Fault-Tolerant Nanocircuits in QCA," *International Scholarly Research Notices*, vol. 2013, pp. 1-9, 2013.

[14] Moallem P., Ehsanpour M., Bolhasani A., Montazeri M., "Optimized Reversible Arithmetic Logic Units," *Journal of Electronics (China)*, vol. 31, no.5, pp. 394-405, 2014.

[15] Gopal L., Syahira N., Mahayadin M., Chowdhury A., Gopalai A., Singh A., "Design and Synthesis of Reversible Arithmetic and Logic Unit (ALU)," *International Conference on Computer, Communications, and Control Technology (I4CT)*, 2014.

[16] Sen B., Dutta M., Goswami M., Sikdar B., "Modular Design of Testable Reversible ALU by QCA Multiplexer with increase in Programmability," *Microelectronics Journal*, vol. 45, no. 11, pp. 1522-1532, 2014.

[17] Thakral S., Bansal D., "Fault Tolerant ALU using Parity Preserving Reversible Logic Gates," *International Journal of Modern Education and Computer Science*, vol, 8, no. 8, pp. 51-58, 2016.

[18] Sasamal T., Singh A., Mohan A., "Efficient Design of Reversible ALU in Quantum-Dot Cellular Automata," *Optik*, vol. 127, no. 15, pp. 6172-6182, 2016.

[19] Krishna Murthy M., "Design of Efficient Adder Circuits Using Proposed Parity Preserving Gate (PPPG)," *International Journal of VLSI Design & Communication Systems*, vol. 3, no. 3, pp. 83-39, 2012.

[20] Thakral S., Bansal D., Chakarvarti S., "Implementation and Analysis of Reversible logic Based Arithmetic Logic Unit," *TELKOMNIKA Telecommunication Computing Electronics and Control*, vol. 14, no. 4, 1292-1298, 2016.

[21] Misra N. K., Wairya S., & Singh V. K., "Approach to Design a High-Performance Fault-Tolerant Reversible ALU," *International Journal of Circuits and Architecture Design*, vol. 2, no. 1, pp. 83-103, 2016.

[22] Gadim M. R., Navimipour N. J., "A New Three-Level Fault Tolerance Arithmetic and Logic Unit Based on Quantum Dot Cellular Automata," *Microsystem technologies*, vol. 24, no. 2, pp. 1295-1305, 2018.

[23] Bahadori G., Houshmand M., Zomorodi-Moghadam M., "Design of a Fault-Tolerant Reversible Control Unit in Molecular Quantum-Dot Cellular Automata," *International Journal of Quantum Information*, vol. 16, no. 1, 2018.

[24] Das B. and Chandran S., "Towards the Designing of Efficient Computing Reversible Fault Tolerant Arithmetic Circuits and ALU," *European Journal of Scientific Research*, vol.150, no. 2, pp. 126-151, 2018.

[25] Thakral S., and Bansal D., "Fault Tolerant Arithmetic Logic Unit," *International Conference on Emerging Current Trends in Computing and Expert Technology*, pp. 226-233, 2019.

[26] Thakral S., and Bansal D., "Improved Fault Tolerant ALU Architecture," *International Journal of Engineering and Advanced Technology (IJEAT)*, vol. 8, no. 6, pp. 1477-1484, 2019.