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Graphene field-effect transistor simulation with TCAD on top-gate dielectric influences

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Abstract

This paper presents the influence of top-gate dielectric material for graphene field-effect transistor (GFET) using TCAD simulation. Apart from silicon-based dielectric that is typically used for top-gate structure, other high-dielectric constant (high-k) dielectric materials namely aluminum oxide and hafnium oxide are also involved in the analysis deliberately to improve the electrical properties of the GFET. The unique GFET current-voltage characteristics against several top-gate dielectric thicknesses are also investigated to guide the wafer fabrication engineers during the process optimization stage. The improvement to critical electrical parameters of GFET in terms of higher saturation drain current and greater on/off current ratio shows that the use of high-k dielectric material with very thin oxide layer is absolutely necessary.

Keywords: *ambipolar characteristics, graphene FET (GFET), high-k dielectric, monolayer graphene, TCAD simulations*

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1. Introduction

Technology scaling of CMOS transistor is approaching its physical limit and GFET is promoted to be one of the worthy candidates with respect to its advanced material properties. This is started with the breakthrough work by Geim and Novoselov in GFET fabrication and characterization using mechanical exfoliation method, which later managed to win the Nobel Prize in Physics 2010 [1-3]. Besides mechanical exfoliation, other methods typically used for graphene synthetization are thermal chemical vapor deposition (CVD) and sublimation of silicon carbide (SiC) where each of these methods contains its own advantages and disadvantages. Different synthesis methods will produce different graphene properties which are suitable for certain device and design applications [4, 5].

Large-area GFET is desirable with respect to its real manufacturability prospect, compared to another graphene-based transistor namely graphene nanoribbons (GNR) [6, 7]. However large-area GFET actually suffer a significance disadvantage with regards to its zero bandgap material properties which contributed to high leakage current and very low ratio of highest on-current (I_{on}) over lowest off-current (I_{off}) [8, 9]. This is also the main reason that has hindered GFET advancement in the forefront digital and analog design applications. Nevertheless manufacturable GFET is still applicable and desired in radio frequency (RF), sensors and detector applications where the ratio of I_{on}/I_{off} is not necessarily significant [10, 11].

Technology Computer-Aided Design (TCAD) is well-known in semiconductor industry as tool for process and device simulations useful for pre-silicon characterizations and optimizations. Although TCAD is loaded with advantages required in technology development phase, there are just minimal reports to be found in literatures linking TCAD with GFET. This is understandably due to the missing graphene material properties in the software and accurate quantum models which require another expensive simulation tool to be integrated to the overall flow for accurate device analysis [12]. In overcoming these obstacles, GFET is simulated with TCAD in the consideration of quantum capacitance effects as reported by Hafsi et al [13]. Besides that, there are works that described the feasibility of GFET simulation with TCAD, by modifying the default material properties, such as bandgap, effective density of states, permittivity and the mobility of the carriers [14, 15].

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On the other hand, top-gate dielectric material is also identified as one of the main parameters which have also contributed to the overall GFET characteristics and performances [16]. There are several dielectric materials available in the semiconductor industry, ranging from classical silicon-based material such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4), to refined high-*k* dielectric material such as aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) [17]. Although there are different literatures reported for different type of dielectric materials used in their GFET structures, there is no thorough analysis provided on the influences of dielectric material based on the same device structure [18, 19].

Considering the importance of critical electrical parameters such as saturation drain current, I_{on} and I_{off} to the different device applications, this paper is focusing on the effect of several top-gate dielectric materials used in GFET structure for electrical parameter's improvements. This work takes the advantages of TCAD simulation to circumvent the laborious, lengthy and costly experiments of real wafer in view of early in-house technology development. The influences of high-*k* dielectric used as a top-gate material on transfer and output characteristic curves are investigated. Electrical characteristics for different top-gate oxide thicknesses are also studied. The outcome would impart a satisfactory guidance to the process engineer in selecting suitable dielectric material and thickness accordingly.

2. GFET Simulation with Sentaurus TCAD

Similar to other transistor's behaviors, GFET is also identified by its transfer and output characteristic curves. But compared to the normal CMOS transistor, GFET is unique because its transfer characteristic or drain current versus gate voltage (I_d-V_g) plot shows an ambipolar behavior where single device is represented by both hole and electron conductions, depending on voltage applied to the gate terminal. The inflection point between these hole and electron conductions is marked by the Dirac voltage (V_{Dirac}) which also represents the maximum resistance and minimum current. As a zero bandgap material, the graphene layer in the transistor's channel cannot be turned off as the leakage current is just too high. For output characteristic curves or drain current versus drain voltage (I_d-V_d) plot, some literatures reported that no saturation current could be generated due to high contact resistances while some observed a mild saturation region [8, 19]. Either with or without mild saturation current value, it is actually another major drawback to GFET as it cannot be used for the high speed applications of digital and analog designs.

In mimicking the complete GFET fabrication flow, Sentaurus TCAD software from Synopsys was utilized in this work as it contains both process and device simulations [20]. For process simulation, there are several fabrication steps involved as simplified in Figure 1. The initial condition is a p-type boron-doped silicon at $1x10^{15}$ cm^{-3} concentration. Next, silicon dioxide at 300 nm thickness was deposited using diffusion process with dry oxygen at 1000 ˚C for 880 minutes. After that, graphene layer was deposited at 5 nm thickness. From typical process simulation point of view, graphene is not a standard material offered by any TCAD software hence polysilicon was chosen as transistor's channel region for this work. As polysilicon is not a self-doping layer while graphene layer is, arsenic at $5x10^{15}$ cm^{-3} concentration was doped to the polysilicon layer to represent such effect. Then, 3 nm thickness of silicon dioxide was diffused and aligned accordingly to gate structure on top of the graphene layer to represent the GFET's top-gate dielectric layer. For the contact formation, 35 nm thickness of aluminum (Al) was deposited and aligned to the contact mask.

Modification of standard polysilicon material properties is mandatory to really represent the actual monolayer graphene properties to the transistor's channel. For this purpose, particularly with the use of Sentaurus TCAD process platform, several material parameters are involved namely bandgap, carrier mobility, permittivity ratio of graphene and vacuum as well constant mobility, as proposed by Ciarrocchi [21]. For the device time-dependent simulation, the selection of suitable transport models is crucial in order to find the right combination for both recombination and carrier mobility models. In Sentaurus TCAD device simulation, recombination phenomenon is modelled with standard Shockley Read Hall (SRH) model while there are several carrier mobility models available such as Philips unified mobility (PhuMob), high field saturation and normal electric field (Enormal) [22]. Good model combinations are required to get the smooth transfer characteristic curves especially at the V_{Dirac} region which is the transition from hole to electron conductions.

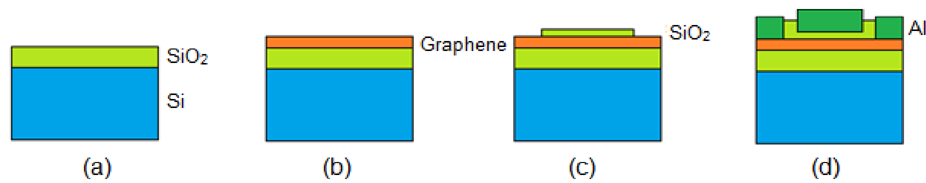


Figure 1. Process flow for GFET TCAD; (a) initial condition, (b) graphene deposition, (c) top-gate oxide deposition, (d) metal contacts

3. Experiment

In the initial stage, the process simulation was carried out using SiO_2 as the top-gate dielectric material. The device simulation results from initial stage were compared with the reported literatures as a benchmarking purpose and supporting the feasibility of the proposed GFET fabrication flow with the TCAD software. Combination of mobility models were tested and verified to achieve the smooth curves of transfer and output characteristics. The I_d-V_g and I_d-V_d curves were also simulated at different channel doping concentrations for qualitative comparison with the benchmark results. Critical electric parameters such as V_{Dirac}, I_{on}, I_{off} and saturation drain current were derived from the device simulation curves. The gate terminal was simulated with the length of 450 nm while the width was fixed at 1 um with respect to the use of two-dimensional (2D) TCAD simulator.

After the completion of benchmarking process using SiO_2 as the top-gate dielectric material, then the experiment was continued with simulation using different dielectric materials namely Si_3N_4, Al_2O_3 and HfO_2. This was done by the direct replacement of material type used during top-gate dielectric deposition step in the process simulation flow. Next the effect of dielectric thicknesses were experimented by reducing the layer thickness from 3 nm to 2 nm and 1 nm, for both SiO_2 and HfO_2 which correspondingly representing silicon-based and high-*k* dielectric materials.

4. Results and Discussion

4.1. Characteristics of SiO_2 as a Top-gate Dielectric

The cross-section of fabricated GFET based on the proposed process flow in Figure 1, using SiO_2 as the top-gate dielectric material is presented in Figure 2. The GFET structure is quite similar to industry standard metal-oxide-semiconductor (MOS) transistor, except the transistor's channel is made of monolayer graphene material.

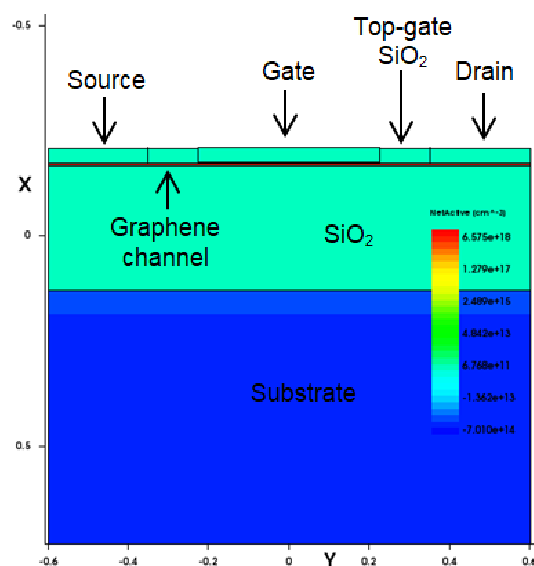


Figure 2. GFET cross-section from sentaurus TCAD process simulations

The simulated transfer characteristic using different combination of mobility models are presented in Figure 3. The results show that the combination of Philips unified (PhuMob) and high field saturation models provide the smoothest curves as compared to other combinations. The inclusion of Enormal mobility model generally contributed to the unnecessary kink effect at the V_{Dirac} point. Therefore only PhuMob and high field saturation models are selected for mobility models while SRH is used for recombination model for the rest of this work.

Figure 4 shows the ambipolar characteristics of I_d-V_g curves for GFET with SiO_2 as a top-gate dielectric material, biased at different drain voltage (V_d). Based on this TCAD simulation works, the most significant graphene properties are the bandgap and carrier mobility where the former is particularly producing the ambipolar curves valid from negative to positive gate voltage (V_g) while the latter is imperative for symmetrical shape of the transfer characteristic curves. It is observed that both I_{on} and I_{off} increase with the increased of V_d while both V_{Dirac} and I_{on}/I_{off} values remain unchanged.

Besides that, I_{on} is decreases with the increased of doping concentration of channel's region as shown in Figure 5 for V_d = 0.2 V. There is a shift of the V_{Dirac}, from -0.72 V to -0.60 V respectively for the doping concentration of $1x10^{15}$ cm^{-3} and $1x10^{19}$ cm^{-3}, which is supporting the idea of tuning the GFET polarity by amending graphene concentration level at certain values [23]. Both outcome of Figure 4 and 5 are critical as benchmarking purposes which are consistent with the results obtained by Johirul et al [9]. The sensitivities of graphene material to voltage and doping concentration variations further promoted its suitability to be well qualified for sensor applications [11].

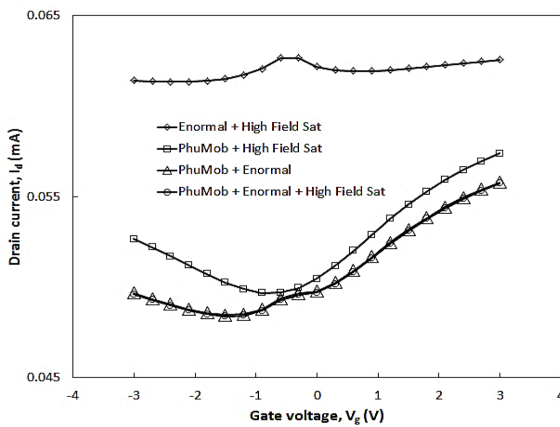


Figure 3. Transfer characteristic curves from different combinations of mobility models

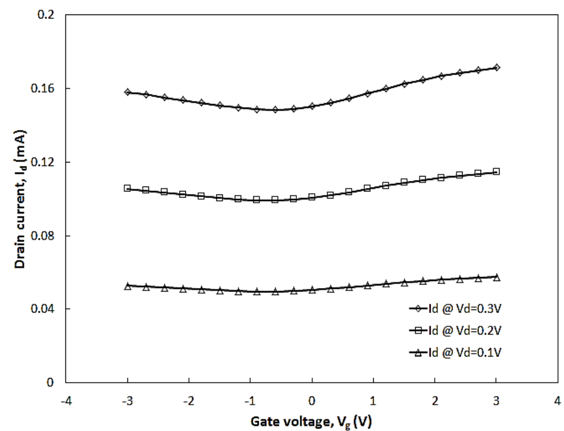


Figure 4. Transfer characteristic curves at different drain voltages (V_d)

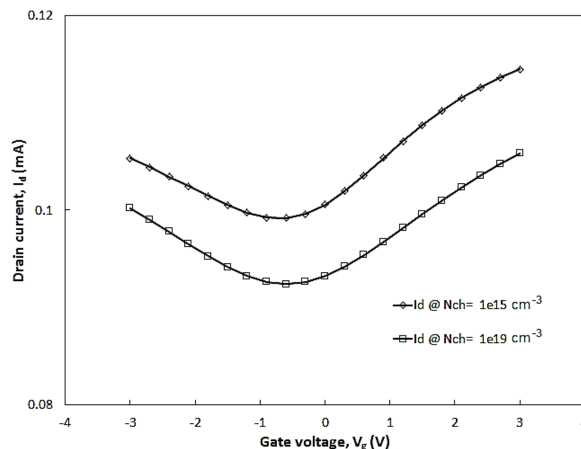


Figure 5. Transfer characteristic curves at different channel doping concentrations

The drain current as a function of drain voltage with different channel doping concentrations and gate voltages is presented in Figure 6. The simulated results show that saturation drain current decreases with increasing channel doping concentration. On the contrary, the saturation drain current increases with increasing biased gate voltage. These results are also qualitatively comparable with the reported data by Johirul and Thingujam et al [14, 15]. It is worth noting that hydrodynamic model is included during the simulation of output characteristic curves in order to increase the accuracies. It slightly increased the simulation time but necessary for normal I_d-V_d curves, or else the fast and simple model simulations end up with unnecessary resistor characteristics.

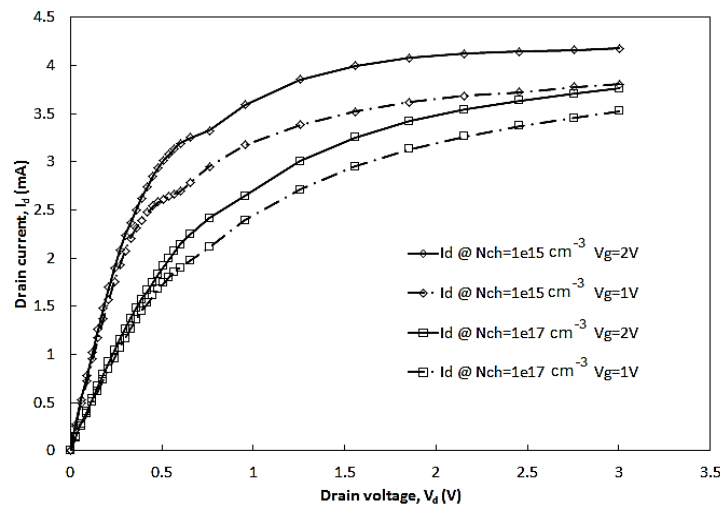
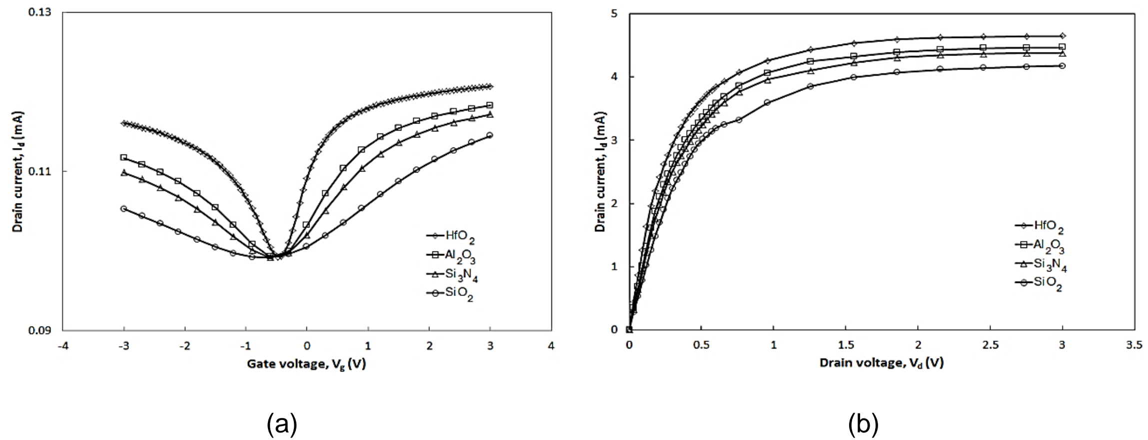


Figure 6. Output characteristic curves at different channel doping concentrations

4.2. GFET Simulations at Various Top-gate Dielectric Materials

The transfer characteristic curves of SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the top-gate dielectric material at film thickness of 3 nm are illustrated in Figure 7 (a). The maximum I_{on} is about 121 uA by using HfO_2 followed by Al_2O_3 and Si_3N_4 as the experimental materials respectively at 118 uA and 117 uA. The lowest I_{on} produced from initial benchmark material of SiO_2 at about 114 uA, which is 6% lower compared to the highest I_{on} value. The results show that the I_{on} value increases with the use of high-*k* top-gate dielectric material where both HfO_2 and Al_2O_3 are superior as compared to silicon-based dielectric of Si_3N_4 and SiO_2. Besides that the use of high-*k* dielectric material also leads to the positive shift of V_{Dirac} from -0.72 V using SiO_2 to -0.48 V using HfO_2. Both Si_3N_4 and Al_2O_3 though shared same V_{Dirac} at -0.54 V. Interestingly all of the top-gate dielectric materials generated about the same value of I_{off} at 99 uA to make the ratio of I_{on}/I_{off} increased from 1.15 of SiO_2 to 1.18, 1.19 and 1.22 correspondingly to Si_3N_4, Al_2O_3 and HfO_2. These results exhibit that the use of HfO_2 is the best option for the overall improvement to the critical electrical parameters such as I_{on} and ratio of I_{on}/I_{off}.

The output characteristic curves of various top-gate dielectric materials used during device simulation experimentations are depicted in Figure 7 (b). Consistent with transfer characteristic curves of Figure 7 (a), the I_d-V_d plot also shows that HfO_2 yielded the highest saturation drain current while SiO_2 produced the lowest saturation drain current. Based on these simulated curves, about 12% improvement of saturation drain current can be observed by replacing the top-gate dielectric material from SiO_2 to HfO_2. These results agree well with current graphene-based transistor's engineering towards the use of high-*k* dielectric material for better device performance [24]. With respect to this distinguished comparison between SiO_2 and HfO_2, the rest of comparisons are done based on these two dielectric materials.



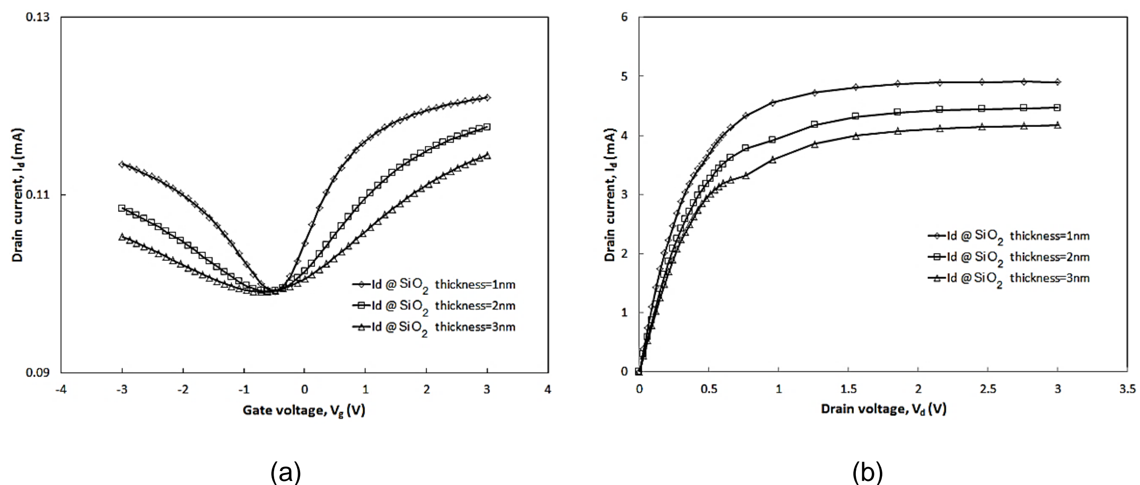
(a) (b)

Figure 7. Simulation curves at various top-gate dielectric materials:
(a) transfer characteristic and (b) output characteristics

4.3. GFET Simulations at Different Top-gate Dielectric Thicknesses

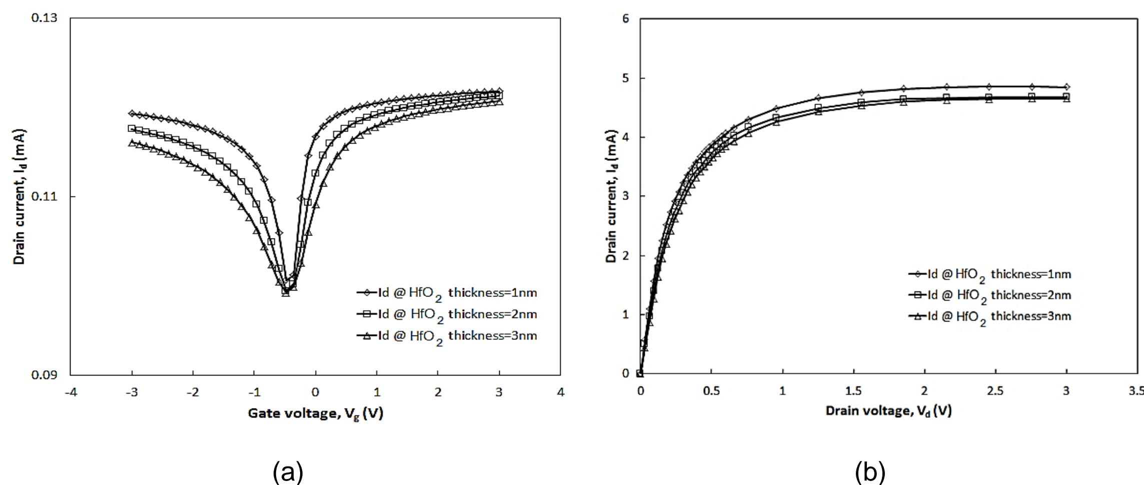
Figure 8 (a) and 8 (b) show the result of device simulations using SiO_2 respectively for transfer and output characteristic curves at different top-gate dielectric thicknesses. For I_d-V_g plot, there is a consistent increase of I_{on} when the dielectric thickness reduced from 3 nm to 2 nm and 1 nm. The results show that I_{on} improves by 6% to 121 uA, as the thickness is reduced to 1 nm. There is also a shift of V_{Dirac} observed from -0.72 V to -0.6 V and -0.48 V when the thickness reduced from 3 nm to 2 nm and 1 nm accordingly. Furthermore, the ratio of I_{on}/I_{off} increases about 6% with reduction of top-gate dielectric thickness from the minimum of 1.15 to the maximum of 1.22 as constant I_{off} value extracted even at different dielectric thicknesses applied. For I_d-V_d plot, the results show that the saturation drain current increases with reduction of dielectric thickness, which is consistent with I_d-V_g plot.

Figure 9 (a) and 9 (b) illustrate correspondingly the I_d-V_g and I_d-V_d characteristics with HfO_2 as the top-gate dielectric material at different dielectric thicknesses. It is seen that I_{on} is slightly increases with the reduction of dielectric thickness for I_d-V_g curves while the saturation drain current rises by 5% to 4.85 mA as the thickness is decreased from 3 nm to 1 nm for I_d-V_d curves. The overall results of HfO_2 simulations are harmonious with previous SiO_2 results which exhibit both silicon-based and high-*k* dielectric materials produce better electrical parameters with the decreasing of dielectric thickness. These attainments also match well with contemporary GFET development in the vicinity of an ultra-thin dielectric material [25].



(a) (b)

Figure 8. Simulation curves at different top-gate dielectric thicknesses for SiO_2:
(a) transfer characteristics and (b) output characteristics



(a) (b)

Figure 9. Simulation curves at different top-gate dielectric thicknesses for HfO_2: (a) transfer characteristics and (b) output characteristics

5. Conclusion

The improvement to the saturation drain current and ratio of I_{on}/I_{off} for GFET characteristics were successfully evaluated using TCAD simulations under varying top-gate dielectric materials and thicknesses. The high-*k* dielectric material has been investigated where the replacement of SiO_2 to HfO_2 shows an improvement in saturation drain current about 12%. The outcomes also reveal that the replacement to HfO_2 improves the ratio of I_{on}/I_{off} about 6% compared to SiO_2. For the variations of dielectric thickness, the ratio of I_{on}/I_{off} increased by about 6% when dielectric thickness was reduced from 3 nm to 1 nm for SiO_2 material, which provides option for silicon-based dielectric refinement. These consequences are precious for the process engineers in determining the suitable top-gate dielectric material with related thickness for actual process fabrications with respect to the available optimized recipes and equipment.

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