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128 mA CMOS LDO with 108 dB PSRR at 2.4 MHz frequency

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Abstract

A low dropout (LDO) voltage regulator with high power supply rejection ratio (PSRR) and low temperature coefficient (TC) is presented in this paper. Large 1µF off-chip load capacitor is used to achieve the high PSRR. However, this decreases the gain and pushes the LDO's output pole to lower frequency causing the circuit to become unstable. The proposed LDO uses rail-to-rail folded cascode amplifier to compensate the gain and stability problems. 2nd order curvature characteristic is used in bandgap voltage reference circuit that is applied at the input of the amplifier to minimize the TC. The characteristic is achieved by implementing MOSFET transistors operate in weak and strong inversions. The LDO is designed using 0.18 µm CMOS technology and achieves a constant 1.8 V output voltage for input voltages from 3.2 V to 5 V and load current up to a 128mA at temperature between -40 °C to 125 °C. The proposed LDO is targeted for RF application which has stringent requirement on noise rejection over a broad range of frequency.

Keywords*: high PSRR, low dropout (LDO) regulator, low temperature coefficient, power management, rail-to-rail folded cascode amplifier*

1. Introduction

Recent advances in system-on-chip (SoC) applications and technology scaling have led to the development of large integration of analog, digital and RF circuit blocks on to a single chip. Technology scaling will affects the performance of these circuit blocks in sense of energy consumption, area of a circuit, speed and delay constraint [1]. Technology scaling benefits the digital circuitry as it significantly lowers the cost of digital logic and memory and minimizing the power consumption [2]. The downside of it is that it has not been suitable to the analog and RF circuit blocks. The decrease in power supply in technology scaling causing the noise on the power supply to become crucial for analog and RF circuits [2]. This is especially true for higher frequency applications. Small ripple from input supply can give quite big impact to the performance of RF circuits and in worst case situation it can cause the circuit to malfunction. For these reasons, low drop-out (LDO) voltage regulator with high noise/ripple rejection at the input supply over a broad range of frequency is very important to provide a reliable and robust output DC voltage. Noise rejection at input supply or mostly known as power supply rejection ratio (PSRR) is defined as the ratio of the change in output voltage to the change in supply voltage.

LDO voltage regulator or LDO is a power management system that is used to generate a stable and constant DC voltage under variations of input voltage, load current and temperature. LDO comprises a voltage reference circuit, error amplifier, pass transistor, and sampling resistor as illustrated in Figure 1 [3]. Large external capacitor and small equivalent series resistor (R_{esr}) is usually used for stability compensation [4]. Sampling resistor is formed by voltage divider network where the input of error amplifier is connected to the resistor network creating a feedback loop. LDO without a feedback network will produce an output identical to the reference voltage (V_{REF}). The purpose of feedback network is for the LDO to produce a desired constant DC voltage. The ratio of feedback network is defined by (1). The error amplifier is used to sense the difference between the feedback voltage (V_F) and the reference voltage (V_{REF}) and amplifies the difference. If $V_F < V_{REF}$, the amplifier will pull lower the gate

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voltage of pass transistor, allowing more current to pass and increasing the output voltage. If $V_F > V_{REF}$, the amplifier will pull higher the gate voltage, limiting the output current thus reducing the output voltage [5].

$$\frac{R1+R2}{R2} V_{REF}=VOUT \quad (1)$$

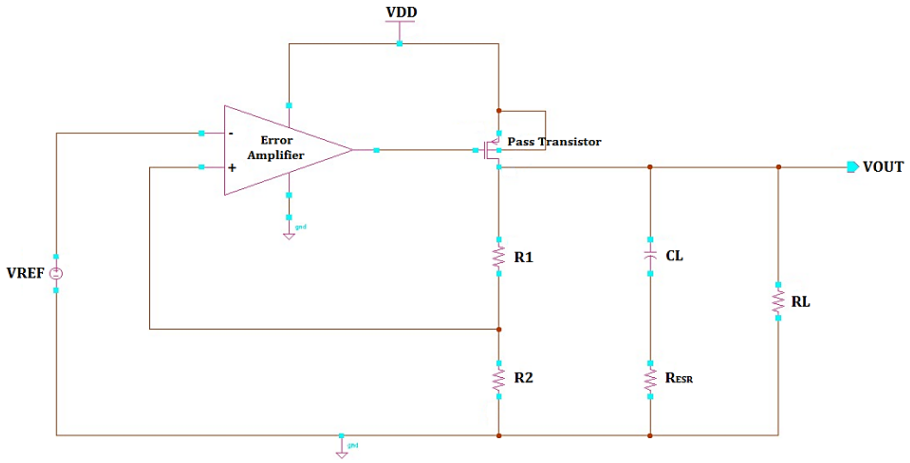


Figure 1. LDO circuit diagram

At high frequency application, the PSRR is mainly influenced by the output capacitor and the ability of the output amplifier to drive the pass transistor [6]. Large capacitor is needed to obtain high PSRR. However, this causing the open-loop gain to decrease and pushes the output pole of the LDO to lower frequency causing the phase margin to decrease and unstable at high frequency. High open-loop gain and phase margin at wide frequency range error amplifier is needed to compensate for this problem. Other than high PSRR, few important parameters also need to be considered including temperature dependence or temperature coefficient (TC), line and load regulations, drop-out voltage and quiescent current (I_q) [7]. This paper is organized as follows: section 2 discusses the design and characteristics of the proposed LDO; section 3 presents the simulation results and discussions of the proposed LDO followed by the conclusion in section 4.

2. Proposed LDO Regulator

2.1. Rail-to-rail Folded Cascode Error Amplifier

Figure 2 illustrates the error amplifier of the proposed LDO. The amplifier has a complementary N- and P-channel pairs formed by M1, M2, and M3, M4 for the LDO to operates at wide range input voltage while achieving high common-mode rejection ratio (CMRR) and low input offset voltage [8, 9]. CMRR tells how well a differential input amplifier rejects noise that is common to the inputs. By having high CMRR, large unwanted noise is rejected by the inputs and allowing only small noises to pass at the output amplifier. Rail-to-rail amplifier has better CMRR due to the wide common-mode range the amplifier has.

The input of the error amplifier is connected to high impedance folded cascode stage to achieve high gain amplifier. Wide swing current mirror is applied to the cascode stage to increase the signal swing in the current mirror. Class AB, rail-to-rail output (M32 and M33) formed a power noise cancellation thus minimizing the size of the pass transistor and increases the power efficiency [10]. Since the amplifier is responsible to drive the gate of the pass transistor which is naturally capacitive, class AB output is also used to reduce the output impedance of the error amplifier to ensure stability of the circuit [11, 12]. The rail-to-rail input and output of the amplifier also allows the LDO to achieve maximum current efficiency and high PSRR, high slew rate and low quiescent current [10, 13, 14]. The amplifier is compensated by capacitor C_{C1} and C_{C2}.

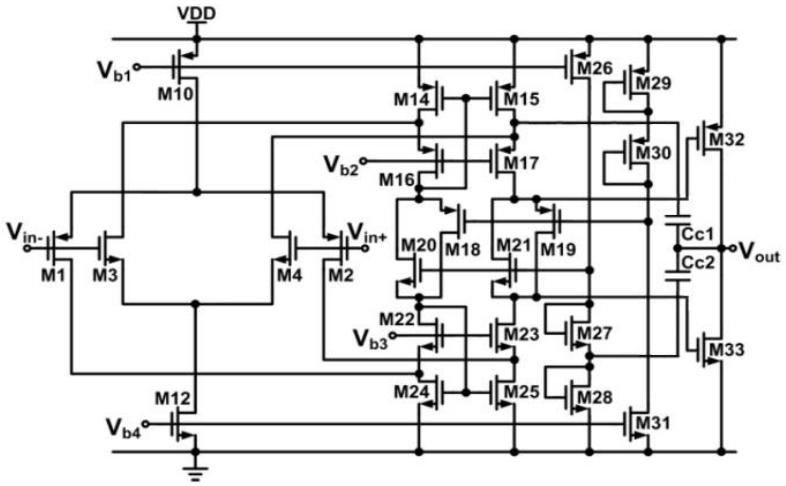


Figure 2. Proposed error amplifier (EA)

2.2. 2nd Order Curvature Bandgap Voltage Reference

Bandgap voltage reference (V_{REF}) circuit is used in LDO to supply constant voltage that is independent to temperature and supply voltage to the error amplifier. Two important factors in V_{REF} are TC and PSRR. TC is defined as resistance-change factor per degree Celsius of temperature change. A quality LDO requires V_{REF} that has low TC and high PSRR to ensure high accuracy regulated output is achieved when there is a change in the temperature or supply voltage. Figure 3 (a) shows the conventional bandgap voltage reference circuit. Bandgap reference comprises two types of voltage: voltage proportional-to-absolute-temperature (V_{PTAT}) and voltage complementary-to-absolute-temperature (V_{CTAT}). The summation of the two voltages produces a constant V_{REF} regardless of temperature change [15]. Due to the non-linearity behavior of the bipolar junction transistor (BJT) the summation of the V_{PTAT} and V_{CTAT} will produce a downward curve voltage. Figure 4 shows the relation of V_{PTAT} and V_{CTAT} to the V_{REF} output voltage. In (2), it shows that thermal voltage (V_T) is proportional to temperature (T) and (3) shows that diode voltage (V_D) possesses both V_{PTAT} and V_{CTAT} where V_{PTAT} is represented by V_T and V_{CTAT} is represented by ln (Io/I_S). I_o and Is are the diode's current flow and reverse bias saturation current respectively. To produce a V_D that has only V_{PTAT}, the V_{CTAT} need to be canceling out. Assuming there is another diode known as V_{D1} that has voltage as shown in (4). By subtracting V_{D1} from V_D, the produced voltage is equals to V_T ln (*N*) where *N* is a number of diode. Thus V_{PTAT} can be achieved.

$$V_T = \frac{kT}{q} \quad (2)$$

$$V_D = V_T\,(\ln(I_o/I_S)) \quad (3)$$

$$V_{D1} = V_T\,(\ln(I_o/NI_S)) \quad (4)$$

$$V_D - V_{D1} = I_oR_o = V_T \ln(N) \quad (5)$$

$$V_{R1} = I_oR_1 = (R_1/R_o)\,V_T \ln(N) \quad (6)$$

From Figure 5, assumes $V_D=V_2$, then $I_oR_o=V_D–V_{D1}=V_T$ ln (*N*) which is the V_{PTAT}. Thus, V_{PTAT} is equals to the voltage across the resistor R_o, and V_{CTAT} is the voltage across the diode, D_1. From (6), the voltage across the resistor, R_1 as shown in Figure 3 (a) is equals to $V_{PTAT}=V_T \ln(N)$ where R_1/R_o is just a ratio. From this, the final V_{PTAT} is measured at the voltage across R_1 and V_{REF} is equals to the total voltage across the R_1 and Q_3. The current mirror circuit formed by M1-M3 is used to provide equal current to each branch in the circuit.

The 2nd order curvature behavior of bandgap voltage reference can minimize the TC or variation of the V_{REF} with respect to temperature. A V_{REF} circuit achieves the 2nd order

characteristics when it possesses both the downward and upward voltage-temperature curves within the desired temperature range as described in Figure 6 and (7). From Figure 6, the 2nd order characteristic can be achieved through the nonlinearity of the V_{PTAT}^2. At very low temperature, the effect of V_{PTAT}^2 is small and cannot compensate the nonlinearity of V_{BE}, generating a downward curve. At high temperature, the V_{PTAT}^2 influences the voltage reference behaviour, generating an upward curve. As a result, both the downward and upward curves can be achieved. In other words, it can be seen that the purpose of implementing V_{PTAT}^2 is to minimize the effect of V_{BE} or increasing the effect of V_{PTAT} at high temperature to generate the 2nd order effect.

$$V_{REF} = V_{BE} + V_{PTAT} + V_{PTAT}^2 \quad (7)$$

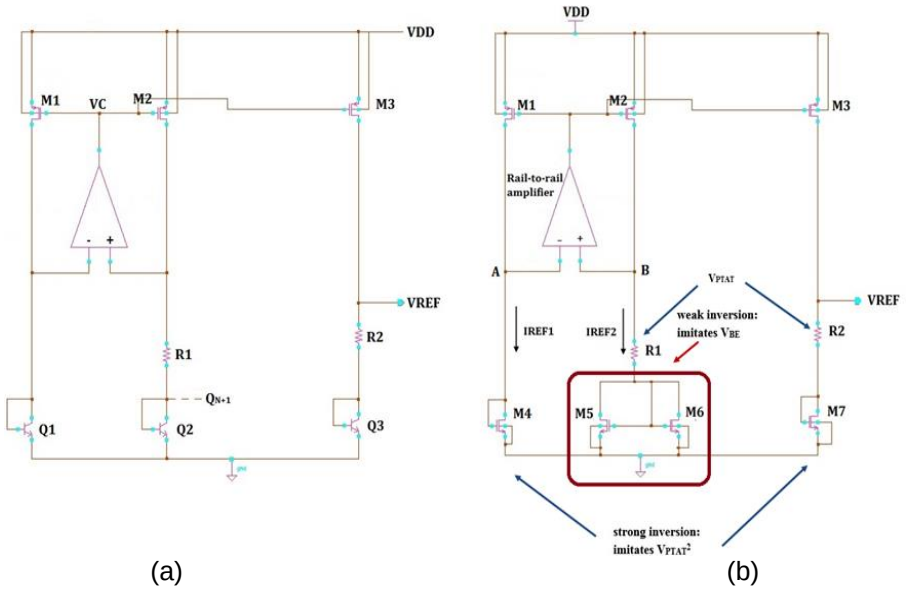


Figure 3. (a) Conventional and (b) proposed bandgap voltage reference

The BJT that is typically used in the voltage reference circuit has negative temperature coefficient and is highly sensitive to temperature. Its V_{BE} decreases with the temperature due to the increase in collector current as the temperature increase. In order to minimize the effect of the V_{BE} the BJT is replaced with MOSFET. In comparison with the BJT, MOSFET transistor that operates in saturation provides positive TC and when applied to the V_{REF} circuit, it will generate an upward curve voltage-temperature characteristic. It is also more thermally stable and is typically smaller than BJT which could reduce the size of core area. The Q3 BJT shown in Figure 3 (a) is replaced with diode-connected MOSFET operates in saturation (M7) to increase the V_{PTAT} effect from R2 as illustrated in Figure 3 (b). The BJT of Q2 that is used to generate and control the V_{CTAT} is replaced with NMOS transistors (M5 and M6) that operate in weak inversion or subthreshold to imitate the characteristics of the BJT. The MOSFET will copy the negative temperature coefficient of BJT thus generating the downward curve at lower temperature. The combination of the two transistors operates in different regions produces a 1st order characteristic at lower temperature and 2nd order characteristic at higher temperature. M4 is designed to operate in saturation to minimize the negative coefficient of M5 and M6 and generates a nonlinear positive temperature coefficient. Polysilicon resistor is used for both R1 and R2 as it has low temperature coefficient compared to diffusion resistor to further reduce the temperature coefficient of the voltage reference [16]. Rail-to-rail amplifier is used in the circuit to achieve high PSRR V_{REF}.

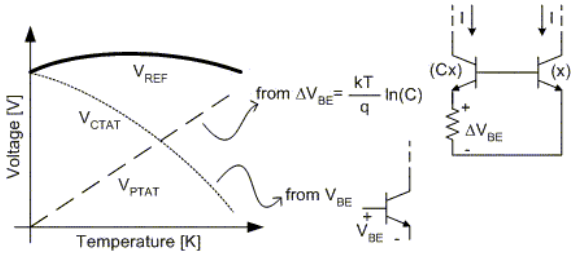


Figure 4. VPTAT (V) and VCTAT (V) vs temperature (°C)

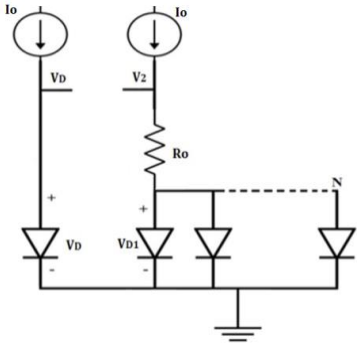


Figure 5. VD and VD1 in bandgap voltage reference

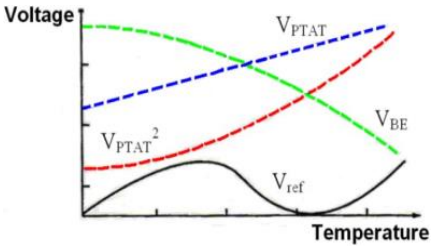


Figure 6. Typical 2nd order curvature bandgap voltage reference [17]

2.3. High PSRR at High Frequency LDO Voltage Regulator

Figure 7 illustrates the PSRR of the LDO can be divided into three regions: low frequency (region 1), mid-range frequency (region 2) and high frequency (region 3) [6]. At region 1, the range starts from DC up to the roll-off frequency of the bandgap reference and the PSRR is determined by the open-loop gain and PSRR of the bandgap voltage reference. Region 2 extends from the bandgap roll-off frequency up to the 0 dB unity gain cross-over frequency. The PSRR is determined from the open-loop gain of the LDO's feedback network which is closely related to the open-loop gain of the error amplifier. Region 3 starts from the 0 dB cross-over frequency to higher frequency where the PSRR is determined by the load capacitor and parasitic elements from the pass transistor along the VDD to the output voltage [6].

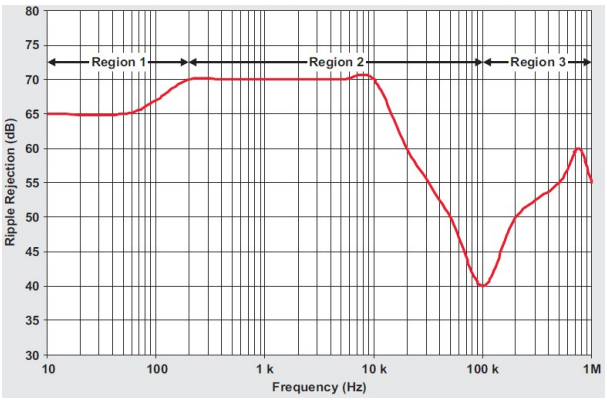


Figure 7. LDO's PSRR curve [6]

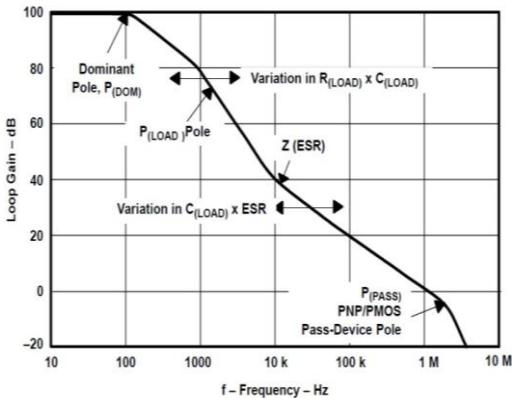


Figure 8. Open-Loop response of typical LDO over frequency [18]

In the proposed LDO, the output load capacitor is made large to achieve the high PSRR at high frequency. However, this costs the LDO's gain and stability. Figure 8 shows the typical

frequency response and location of poles of typical LDO. The dominant pole ($P_{(DOM)}$) is determined by the error amplifier. The load pole ($P_{(LOAD)}$) is formed by the output capacitor and load while the pass-device pole ($P_{(PASS)}$) is defined by the parasitic capacitance of the pass transistor. From the figure, as the $P_{(LOAD)}$ dominates the LDO, the open-loop gain starts to roll-off and pushes the load pole to lower frequency which effectively lowers the 0 dB cross-over frequency and decreases the phase margin. Simplest method to compensate for this problem is to delay the 0 dB cross-over frequency by controlling the frequency compensation of the error amplifier. The compensation capacitors, C_{C1} and C_{C2} of the error amplifier shown in Figure 2 are made large to ensure the phase margin of the LDO is sufficient enough for the circuit to be stable. A stable circuit typically needs at least 60° phase margin. Figure 9 shows the proposed LDO circuit.

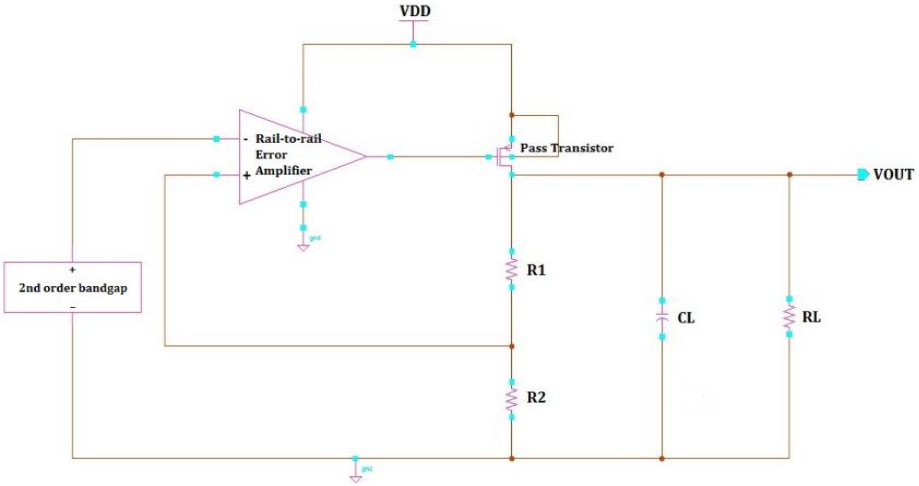


Figure 9. Proposed LDO regulator

3. Results and Analysis

The proposed circuit is designed using thick oxide 0.18 µm Silterra CMOS technology and produce a 1.8 V output voltage at input supply of 3.3 V and temperature between -40 °C to 125 °C. 1.65 V V_{REF} and 10 µA current is injected into the error amplifier to power the circuit. 1 µF off-chip capacitor is applied at the output of the LDO to obtain high PSRR system. The specification of the proposed LDO is tabulated in Table 1.

Table 1. Proposed LDO Specifications

Descriptions	Specifications
Supply Voltage	3.3 V ~ 5 V
Technology	0.18 µm
Temperature	-40 °C ~ 125 °C
Load current	≥ 100 mA
TC	≤ 10 ppm/°C
PSRR	≥ 100 dB
Operating frequency	≥ 2.4 GHz
Line Regulation	5 V/V
Load Regulation	15 mV/V

3.1. Error Amplifier

Figure 10 shows the pre-layout, Monte Carlo and and post-layout simulation results of error amplifier. As mentioned in section 2.1, rail-to-rail folded cascode amplifier provides high open-loop gain. This is proved by the result below. The amplifier obtained 110.7 dB and 83.3° phase margin for the pre-layout simulation and 111.4 dB and 83.38° phase margin for the Monte Carlo simulation at process and mismatch variations analysis. For the post-layout result, the rail-to-rail folded cascode amplifier achieves 110.7 dB open-loop gain and 81.44° phase margin.

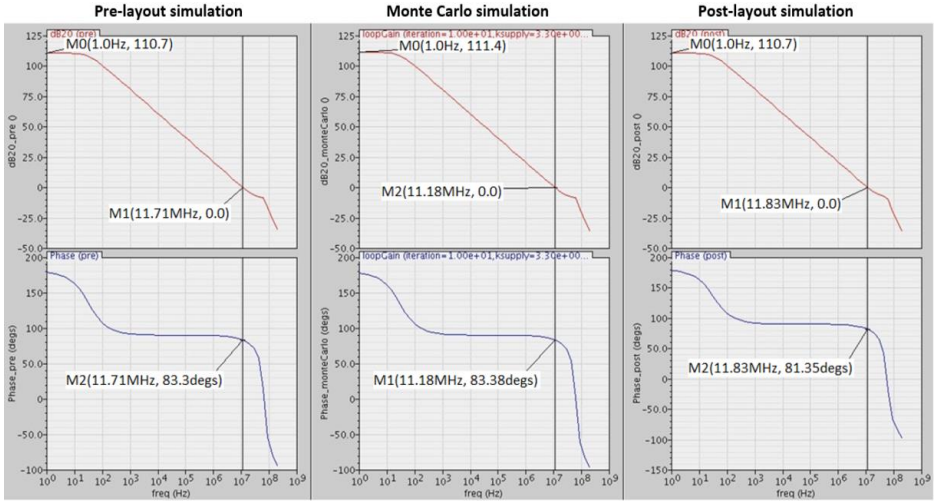


Figure 10. Gain (dB 20) and phase (°) vs frequency (Hz)-pre-layout, Monte Carlo (process and mismatch variations) and post-layout simulations of error amplifier

3.2. Bandgap Voltage Reference

Figure 11 shows the pre- and post-layout simulation results as well as Monte Carlo in process and mismatch variations analysis of V_{REF} when temperature is varied from -40°C to 125°C. The weak and strong inversion MOSFET applied to the bandgap reference allow the circuit to achieve 2nd order curvature voltage-temperature behavior which helps in obtaining low TC. At nominal conditions, the V_{REF} achieves 1.65017 V at room temperature (27°C) and 4.15 ppm/°C TC. At process and mismatch variations analysis (Monte Carlo), the V_{REF} obtained 1.667 V at 27°C and 6.4 and ppm/°C, a slightly higher than the pre-layout simulation in typical condition. From the post-layout simulation result, the total TC obtained by the V_{REF} circuit is equals to 4.3338 ppm/°C.

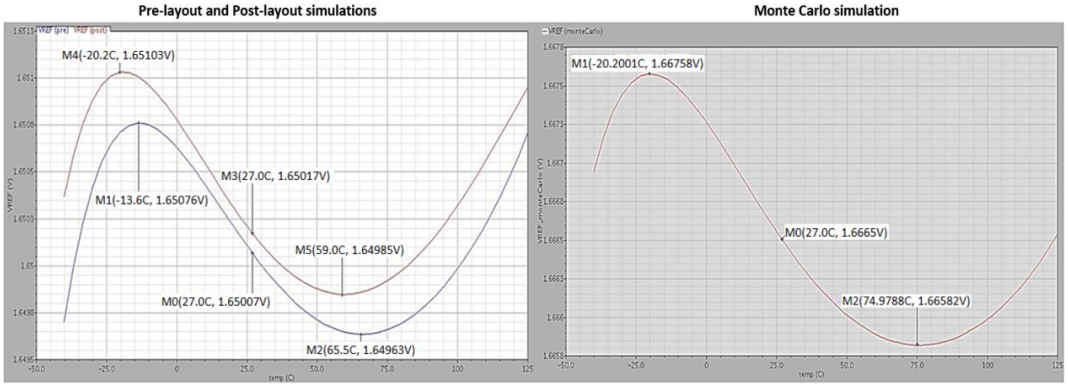


Figure 11. V_{REF} (V) vs Temperature (°C)–pre-layout, post-layout and Monte Carlo (process and mismatch variations) simulations of bandgap voltage reference

3.3. LDO Voltage Regulator

Figures 12–16 show the comparison of pre-layout and post-layout simulation results as well as Monte Carlo in process and mismatch variations analysis of LDO voltage regulator. At 115mA load current, the LDO produces 1.8 V output voltage for both the pre- and post-layout simulations. The LDO in Monte Carlo analysis however obtained 1.847 V at the same load current. The pre-layout LDO able to maintain the 1.8 V output voltage for load between 0mA to 156.8mA and at supply voltage between 2.9 V to 5 V as depicted in Figure 13. However, due to parasitic capacitance and resistance that exists in the layout of the LDO, the post-layout LDO able to maintain its 1.8 V output DC for maximum load current of 128.8mA and supply between

3.2 V to 5 V only. The LDO in Monte Carlo simulation when process and mismatch variations are considered, maintained its constant output for load between 0 mA to 154.8 mA. From Figure 13 (a), the post-layout LDO obtained 1.2944 mV/V line regulation and 11.88 mV/A load regulation as measured in Figure in 13 (b). The LDO achieves very high 108.4 dB PSRR at 2.4 GHz operating frequency as illustrated in Figure 14. This shows that the LDO is suitable for high frequency application. Considerable 70.5 dB gain and 75.76° phase margin are measured from the open-loop LDO as shown in Figure 15. Due to the very small TC provided by the V_{REF} circuit, the post-layout LDO also has small TC which is 4.2417 ppm/°C only as measured from Figure 16. The total core area of the proposed LDO is 1499 µm x 1127.385 µm as depicted in Figure 17. The proposed LDO achieves high PSRR in high operating frequency as shown in Table 2.

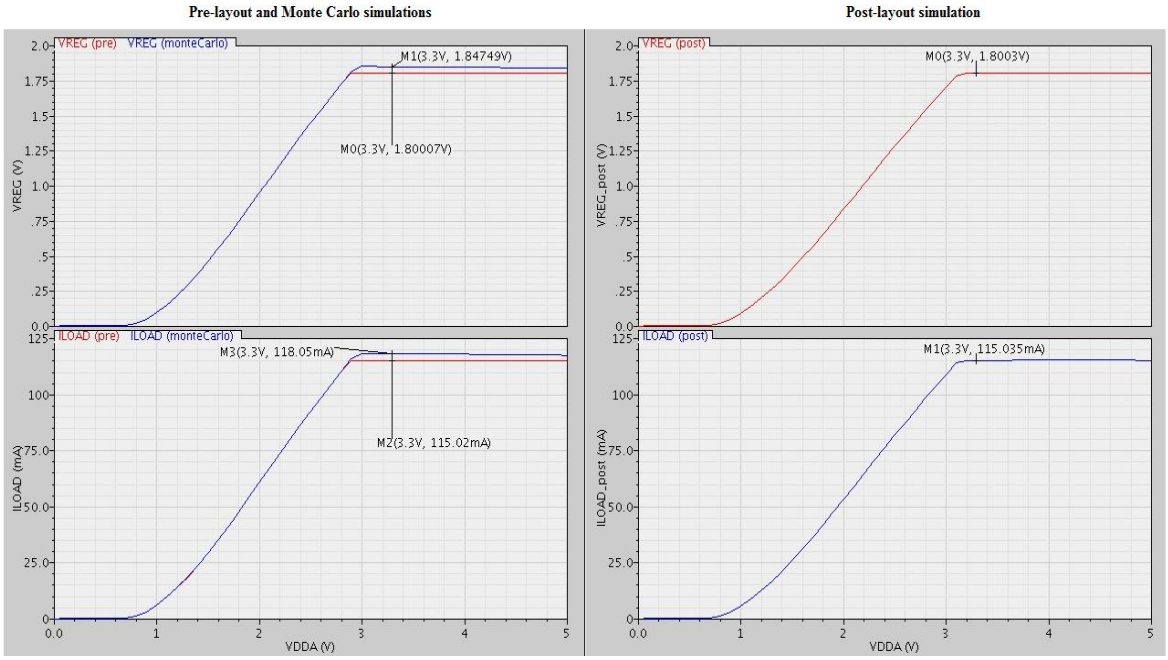
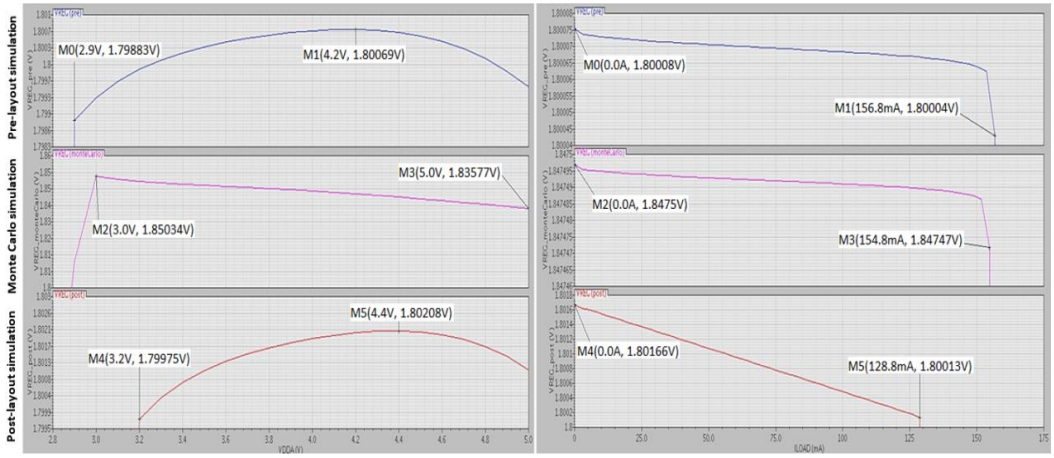


Figure 12. Regulated voltage, V_{REG} (V) and ILOAD (mA) vs Supply voltage, VDDA (V)–pre-layout, Monte Carlo (process and mismatch variations) and post-layout simulations of LDO



(a) (b)

Figure 13. (a) Static line regulation and (b) Static load regulation–pre-layout, Monte Carlo (process and mismatch variations) and post-layout simulations of LDO

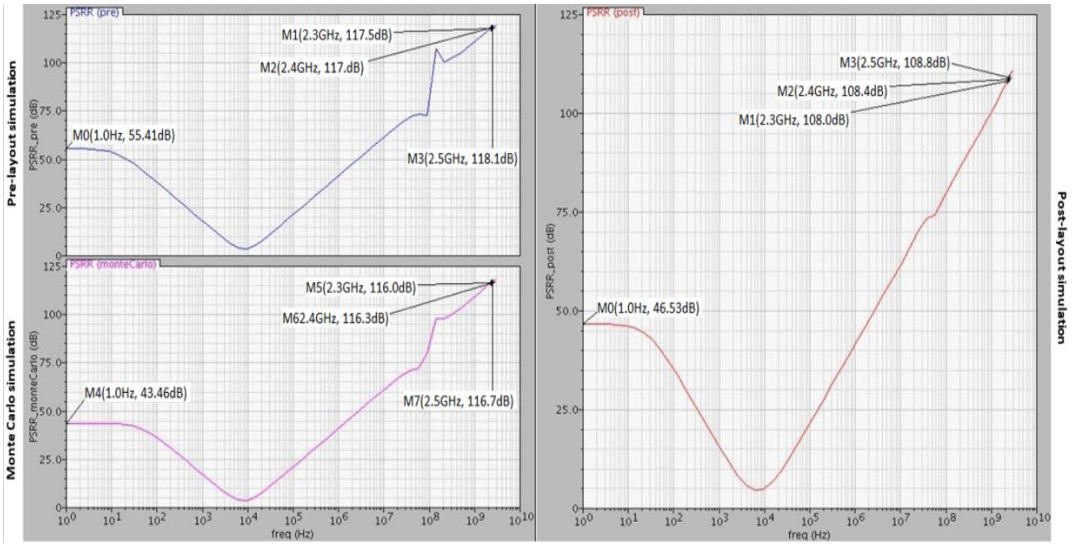


Figure 14. PSRR (dB 20) vs frequency (Hz)–pre-layout, Monte Carlo (process and mismatch variations) and post-layout simulations of LDO

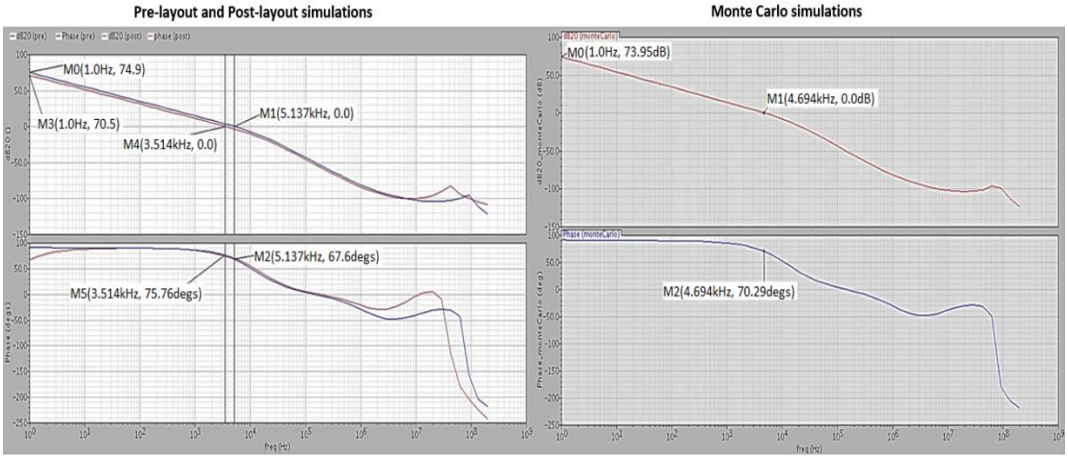


Figure 15. Gain (dB 20) and phase (°) vs frequency (Hz)–pre-layout, post-layout and Monte Carlo (process and mismatch variations) simulations of LDO

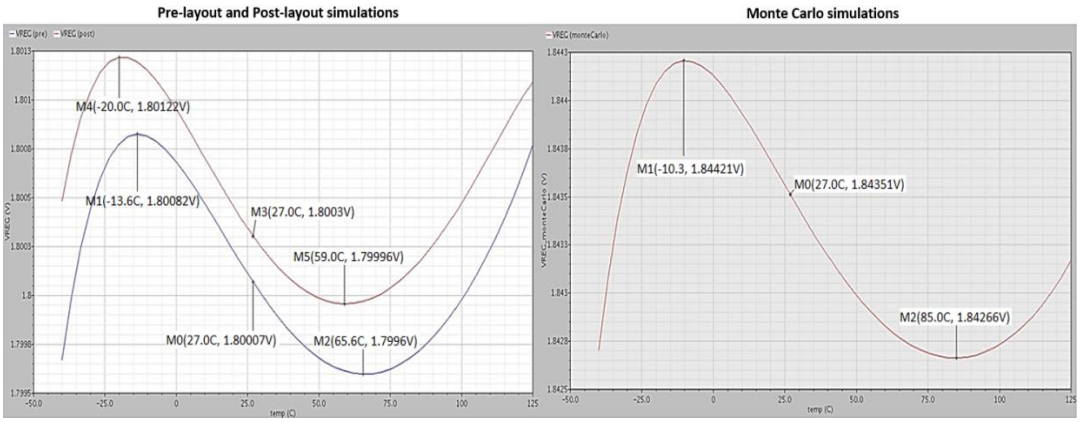


Figure 16. Regulated voltage, V_{REG} (V) vs temperature (°C)–pre-layout, post-layout and Monte Carlo (process and mismatch variations) simulations of LDO

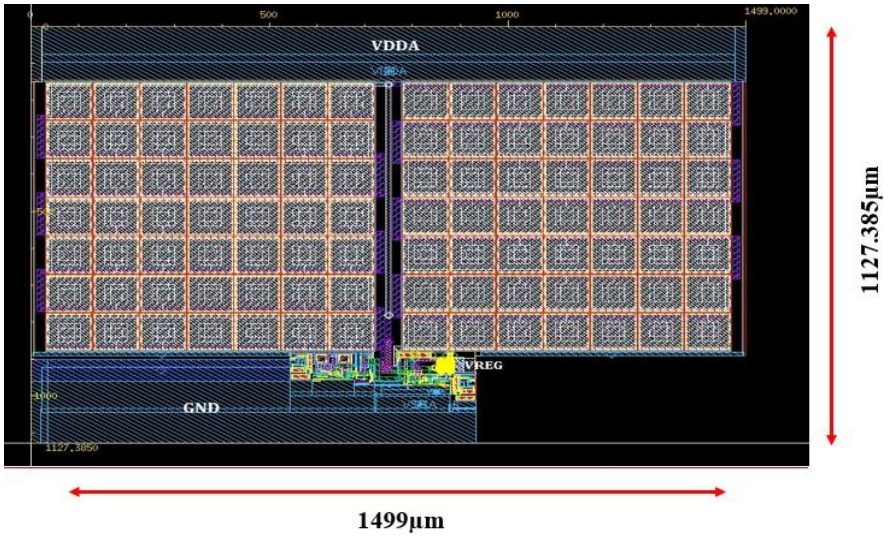


Figure 17. Layout diagram of the proposed LDO circuit

Table 2. LDO Voltage Regulator Performance Benchmarking

Topology	[19]	[20]	[21]	[22]	[23]	[24]	[25]	This Work Pre-layout	This Work Post-layout
Year	-	2010	2012	2013	2013	2015	2016	2018	
Technology	0.35 µm	0.18 µm	0.18 µm	0.18	0.18 µm	90 nm	0.18 µm	0.18 µm	
Supply voltage (V)	5	2	3.3-5.5	1.8-3.6	-	1	1.8	2.9-5	3.2-5
Load current max. (mA)	100.1	300	50	50	40	1	200	156.8	128.8
Load Capacitor (C_L)	35 nF	-	12 pF	24	Capacitor-less	1 µF	-	1 µF	
Regulated voltage, (V_{REG}) (V)	4.507	1.8	1.2	1.6	1.2	0.0932	1.25	1.8	
Line regulation (mV/V)	3.2	0.025	-	0.26	-	7.41	-	0.8857	1.2944
Load regulation (V/A)	0.012	0.9 m	-	0.6	-	0.11	0.8 m	0.25 m	11.88 m
PSRR (dB) @ frequency (Hz)	34.31 @ 10K	50 – 55 @ 100M	60 @ 10K	41 @ 1M	22 – 24 @ 1G – 10G	-	46 - 48 @ 2G - 3G	117.8 @ 2.4G	108.4 @ 2.4G

4. Conclusion

A high PSRR voltage regulator has been designed using 0.18 µm thick oxide Silterra Technology. The circuit is powered by 3.3 V supply voltage to produce an output of 1.8 V regulated voltage. High open-loop gain rail-to-rail folded cascode amplifier is used in the voltage reference and LDO voltage regulator circuits to obtain low TC and high PSRR system at high frequency operation. The LDO achieves 108.4 dB PSRR at 2.4GHz operating frequency and 4.2417 ppm/°C TC for temperature between -40°C to 125°C.

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