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A 9.38-bit, 422nW, high linear SAR-ADC for wireless implantable system

Silpa Kesav Velagaleti[1], Nayanathara K. S.[2], Madhavi B. K.[3]
[1,2]Department of Electronics & Communication Engineering, CVR College of Engineering, Hyderabad, India
[3]Department of Electronics & Communication Engineering, Siddhartha Institute of Engineering & Technology, Hyderabad, India

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ABSTRACT

In wireless implantable systems (WIS) low power consumption and linearity are the most prominent performance metrics in data acquisition systems. successive approximation register-analog to digital converter (SAR-ADC) is used for data processing in WIS. In this research work, a 10-bit low power high linear SAR-ADC has been designed for WIS. The proposed SAR-ADC architecture is designed using the sample and hold (S/H) circuit consisting of a bootstrap circuit with a dummy switch. This SAR-ADC has a dynamic latch comparator, a split capacitance digital to analog converter (SC-DAC) with mismatch calibration, and a SAR using D-flipflop. This architecture is designed in 45 nm CMOS technology. This ADC reduces non-linearity errors and improve the output voltage swing due to the usage of a clock booster and dummy switch in the sample and hold. The calculated outcomes of the proposed SAR ADC display that with on-chip calibration an ENOB of 9.38 (bits), spurious free distortion ratio (SFDR) of 58.621 dB, and ± 0.2 LSB DNL and ± 0.4LSB INL after calibration.

Corresponding Author:

Silpa Kesav Velagaleti
Department of Electronics & Communication Engineering
CVR College of Engineering
Mangalpally, Hyderabad, India
Email: shilpakesav@mail.com

1. INTRODUCTION

Successive approximation register (SAR)-analog to digital converters (ADCs) are one of the foremost methods for comprehending ADCs converters because of their medium speed, medium accuracy, and moderate circuit complexity [1]. Such converters are widely utilized in the wireless implantable systems (WIS) as shown in Figure 1. WIS protocols have been recently widely adopted for biomedical imaging and sensing applications such as optical coherence tomography [2-4]. The blocks in the wireless implantable systems are micro-electronic array, high gain instrumental amplifier, extremely truncated power ADC, microprocessor unit, transceiver and power provide components. The neural signals are identified by microelectrode array and these signals are amplified by an instrumentation amplifier. These amplified signals are converted into digitalized signals by SAR-ADC. All types of arithmetic and logical operations are done by the microprocessor unit (MPU) which produces a digital version of the neural signals. These digital signals are processed in computers with the help of RF transceiver. In this wireless implantable system, ADC plays a vital role in the conversion of analog signals into digital with enough accuracy. Most of the ADCs and switched capacitor filters [1] need a considerable process in achieving high linearity [5], high precision [6] plus a minimal power dispersing in

low supply voltages. To decrease the overall power consumption [7-10], a single-ended SAR ADC may be a favorite solution.

The contribution of this research paper is a split capacitance digital to analog converter (DAC) with on-chip calibration to reduce area and power dissipation. The most authentic things influencing the linearity of the SAR-ADC are charge injection and clock feedthrough. A couple of solutions are proposed to overcome the newly referenced issues. A standout amongst the foremost generally utilized is the dummy switch technique and transmission gate method. The total design is simulated in Cadence 45 nm CMOS technology at a typical (TT) process corner. These concepts are explained in the following sections. This research paper is structured as follows: section 2 depicts the basic building blocks and proposed techniques of SAR ADC. Section 3 presents the experimental outcomes. Conclusions are given in section 4.

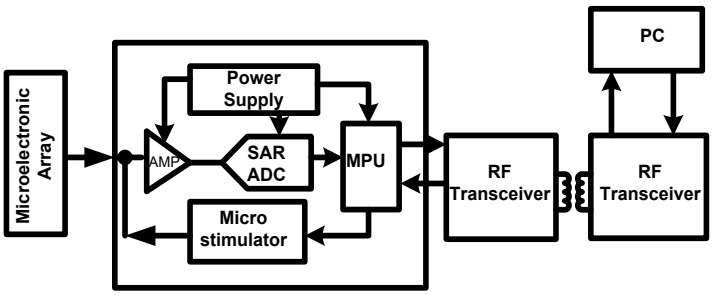

Figure 1. The block diagram of wireless implantable system [11]

2. IMPLEMENTATION OF SAR-ADC

To achieve high accuracy with reduced non-linearity errors, a bootstrap circuit with a dummy switch has been proposed in a fully differential manner. The Architecture of the suggested SAR-ADC is demonstrated in Figure 2. The fully differential structure at the front-end of ADC reduces the substrate, supply noise, and common mode noise. In this architecture split capacitor, DAC with calibration is used to lessen the capacitor mismatch and power dissipation. In this proposed ADC sampling is done on the capacitor's top plates through the bootstrap switch [12]. Voltage V_{ref} is directly connected to the bottom plate of the capacitor through control logic. The dynamic latch comparator compares the initial value without shift up any capacitor. Determined by the inherent logic of this comparator that the MSB capacitor is changed into the ground. The process will be replicated until the right LSB has been decided. The elementary blocks of this proposed ADC are sample and hold, dynamic latch comparator, successive approximation register, control logic, and DAC. There are two non-ideal effects associated with the bootstrap switch at the front-end of ADC. These two impacts are charge injection and clock feedthrough. These non-ideal effects and can be reduced by the clock booster circuit, the dummy switch method in the bootstrap circuit. The usage of split capacitance DAC gives mismatch error. Therefore, to reduce those mismatches on-chip calibration has been done and presented in this paper.

2.1. Clock booster operation

The conductance is required to maintain the linearity of any circuit. The conductance of this switch is not continuous. It hangs over the 3 terminals of MOSFET and available on principal source voltage. Thus, to modulate the output with fewer distribution voltages, signals beyond the distribution voltage scale is desirable. This type of application may be reached using the clock booster. In this section description of the bootstrap circuit and clock booster is explained. The circuit of the clock booster is displayed in Figure 3. The input clock of the clock booster [5] is given at input Q. In case the input voltage is still high, and then the output signal inverter Qb is likely to be in low voltage, then the output voltage at the second inverter Qd will be high. The node Qd is connected as an input to MOSFET NM0. So, this NM0 MOSFET will be ON. The ground voltage will appear at node a. The MOSFET NM1 gate is attached to the power supply, therefore this NM1 MOSFET will probably be ON all the time. The voltage at output port Q2 is low and this port is connected to the gate of PM0 and PM2. So, these MOSFETs will be ON and pre-charged to Vdd. In case the input clock voltage is low, then the MOSFET PM0 will be at Vdd and PM1 will be at Vdd ¬--Vtp. During this time, the capacitors C1 and C2 will be charged to supply voltage Vdd. The MOSFET PM2 is used to retain the Vgd of PM3 as low and Vgs as Vdd+ Vth,p. The voltage at node Q2 is given by:

$$V(Q\_2)=2\times V\_dd\ (C\_1/(C\_1+C\_2)) \quad (1)$$

The capacitance C2 comprises of the parasitic capacitance on the nodes focused by Q2. To minimize parasitic capacitance C1 is chosen as a very high value. That is . With this value, approximately 2Vdd output voltage will be attained.

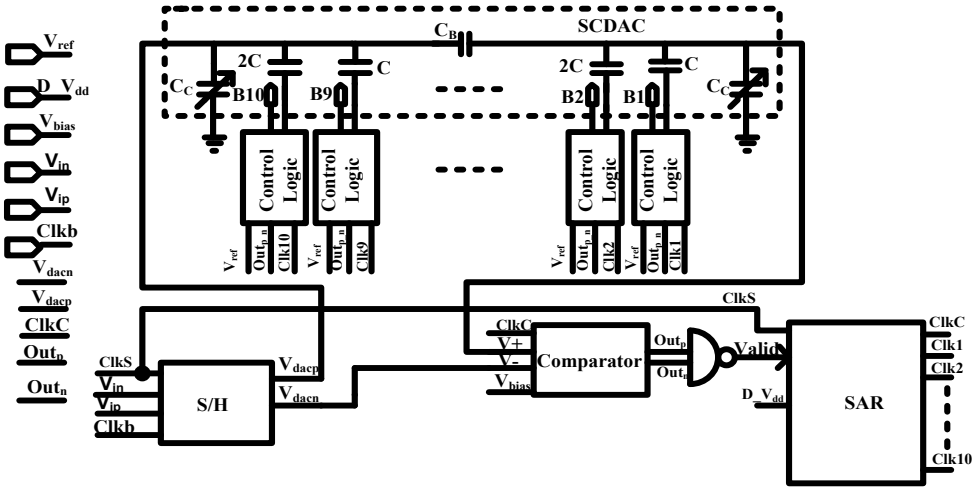

Figure 2. The Shematic of proposed single ended SAR ADC

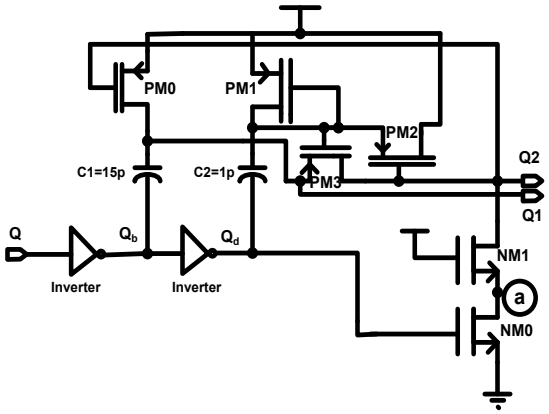

Figure 3. Diagram of clock booster circuit

2.2. The proposed bootstrap circuit

The proposed design with the dummy switch at the output of the bootstrap switch as presented in Figure 4. In this circuit, when Clkb is in high state NM1 will be "ON" and used to store the voltage V_{dd} in the capacitor C by PM1 and NM1. This capacitor acts as a storage capacitor between the V_{gs} of MOSFET NM4. The MOSFETs PM2 and NM3 are utilized to separate the capacitor C from NM4 when the capacitor is charging. At the point when the Clk is in high state, the point NM0 will be "ON" and it pulls down the gate voltage of M2, making PM2 "ON". Presently, the MOSFET PM2 is "ON" and it permits the charge stored in capacitor C into the gate of the MOSFET NM4. The MOSFET NM3 is utilized to keep the gate voltage of NM4 at the supply voltage V_{dd} by making V_{gs} of NM4 as constant. Precisely the stage when the input voltage V_{gs} of this NM4 is currently at V_{dd}, subsequently the gate voltage will likely probably be at $2V_{dd}$. The dummy switch is connected between the bootstrap switch and the output to avoid non-linearity errors. In this sample and hold circuit, clock booster outputs Q1 and Q2 are connected to Clk, Clkb of the proposed bootstrap circuit to regulate the output voltage swing. When NM4 goes to OFF state, half of the channel charge moves towards the switch NM7 and another half of the charge moves towards the input V_{in}. The channel charge per unit area of inverted channel can be written as;

$$Q_I'(y) = C_{ox}'.(V_{GS} - V_{THN}) \quad (2)$$

The total charge in the channel must then be multiplied by the area of the channel resulting in;

$$Q_I(y) = C'_{ox}.W.L.(V_{GS} - V_{THN}) \quad (3)$$

Therefore, the change in voltage across the C_{load} of the NMOS switch is;

$$\Delta V_{load} = -\frac{C'_{ox}.W.L.(V_{DD}-V_{in}-V_{THN})}{2C_{load}} \quad (4)$$

If the clock swings between V_{dd} and ground and by substituting the threshold voltage, then V_{load} is;

$$\Delta V_{load} = \frac{C'_{ox}.W.L.(V_{DD}-V_{in}-[V_{THN0}+\gamma\sqrt{|2V_{fp}|+V_{in}}}{2C_{load}} - \frac{\gamma\sqrt{|2V_{fp}|}}{2C_{load}} \quad (5)$$

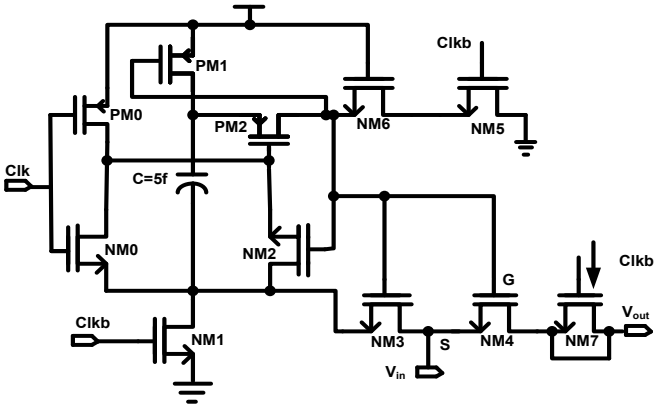

Figure 4. The proposed bootstrap circuit

The change in voltage across C_{load} is non-linear with respect to V_{in} due to the threshold voltage. This non-linearity can be overcome by connecting one NMOS switch with source and drain shorted. The MOSFET NM7 source and drain are short-circuited. Channel can still be established after applying enough voltage at gate control. The charge injected by NM4 will be matched by the charge induced by NM7. Now, if NM7 MOSFET is in the OFF state, then the total charge will be induced in both the directions. Since NM7 source and drain are shorted and V_{in} is a low impedance node, the total charge will be injected into NM4 MOSFET to the input voltage V_{in}. Thus, the non-linearity errors of clock feedthrough and charge injection have been reduced. Therefore, the proposed bootstrap design with dummy switch in the full differential structure of the sample and hold architecture shows the better linearity.

2.3. Dynamic latch comparator

The diagram of the proposed dynamic latch comparator with reduced mismatch [13-15] is shown in Figure 5. This comparator works in two stages, namely, the conversion stage and the regeneration stage. In the conversion stage, the input voltages of the dynamic latch comparator approach to the ground. When ClkC is high the MOSFET M7 is in the cut-off region, then the outputs Out_P and Out_N of the comparator are changed to logic1. After ClkC drives to logic 0, at that time the MOSFETs M5 and M6 are in the cutoff region plus M7 will be turning on. At that time, the comparator is in the comparison phase. To enhance the dynamic latch comparator in terms of offset voltage and power, the mismatches of the differential pair have to be proved first. The PMOS transistors (M1, M2, M7, Mb) are taking the aspect ratio of W/L=4 µm/180 nm, and NMOS transistors are taking the aspect ratio of W/L =2 µm/180 nm and the PMOS inverter pair (M8 and M10) aspect ratio is 3 µm/180 nm. The threshold mismatch V_{th} is $\sigma_{V_{th}} = \frac{AV_{th}}{\sqrt{WL}}$ and the current factor $\beta = \mu_n C_{ox}$ can be expressed as $\sigma_\beta = \frac{A_\beta}{\sqrt{WL}}$. Here AV_{th} and A_β are process parameters. The offset voltage of the dynamic latch comparator can be stated as;

$$V_{os} = \Delta V_{th1,2} + \frac{(V_{gs}-V_{th})_{1,2}}{2}\left(\frac{\Delta M_{1,2}}{M_{1,2}} + \frac{\Delta R}{R}\right) \quad (6)$$

where $\Delta V_{th1,2}$ is the threshold voltage of the input differential pair M1 and M2,$(V_{GS}\text{-}V_{TH})_{1,2}$ is the effective voltage of the differential MOSFETs, $\Delta M_{1,2}/M_{1,2}$ is the mismatch among M1 and M2, ΔR would be the loading resistance discrepancy produced by M3-M6. The primary expression is a change of threshold voltage, which is very less, so this term does not affect the function. Another term is signal reliant on dynamic offset. The MOSFET M12 is used to reduce the mismatch between the MOSFETs M1 and M2. Mismatch parameter is reduced to lessen the Offset voltage, and by using Monte Carlo analysis, the widths of M2 and M7 are measured as 3.68 µm and 3.8 µm respectively. In this design to compare all the combinations of digital to analog converter outputs, the size of this comparator has been taken as minimum width 3 µm and 1 µm respectively.

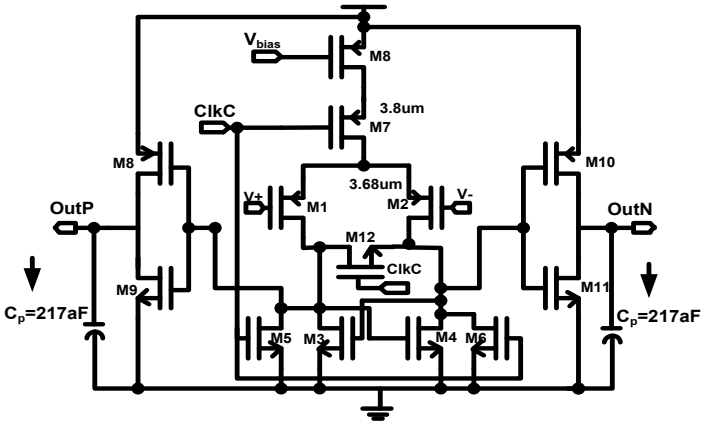

Figure 5. The proposed dynamic comparator

2.4. Split capacitance DAC

Split capacitance charge redistribution digital to analog converter (SC-DAC) is the best method to reduce input capacitance, area, and power. In 10-bit charge redistribution DAC, the total capacitance value is 512C, which occupies a large area and dissipates more power. To reduce input capacitance and power consumption split capacitance array DAC [16-20] has been used. The capacitances are divided into L-side and M-side connected with the bridge capacitor. The lower weight side capacitance is equivalent to the higher weight side capacitance. The bridge capacitor C_b origins poor matching and non-linearity with neighboring capacitors. To improve matching and linearity, an on-chip calibration method with the split capacitance DAC has been proposed. The schematic of DAC with calibration is shown in Figure 6. Initially, for split capacitance DAC, capacitor values are Cn, Cn, 2Cn, 4Cn, 8Cn,16Cn, and bridge capacitance is (32/31)Cn. With these values, the power consumption and non-linearity are more. Hence, the bridge capacitance is C_b is designed to be greater than (32/31)Cn. The calibration capacitance Cc can be implemented on node Q to recompense the mismatch of the split capacitance DAC array. Here, C_{p1} and C_{p2} are the parasitic capacitors. The node P is set to common-mode voltage V_{cm} throughout the sampling phase and it returns to Vcm toward the finish of the conversion phase. In this manner, node P acts as a virtual ground and the parasitic capacitance on this node can be ignored. Assuming that the bottom plates of all L-side capacitors are associated with certain voltage V_x and utilizing the voltage division principle, the voltage at node Q can be determined as follows:

$$V_Q = \frac{32Cn}{32C+C_c+C_{p1}+C_{p2}+C_B}.V_X \quad (7)$$

The charge provided to node P is;

$$Q = (C_B + C_{p2}).V_Q = \frac{(C_B+C_{p2}).32C}{32C+C_c+C_{p1}+C_B+C_{p2}}.V_X \quad (8)$$

Considering the parasitic capacitance, the total weight C_{total} of the L-side capacitors and C_B can be expressed as;

$$C_{total} = \frac{(C_B+C_{p2}).32Cn}{32C+C_c+C_{p1}+C_B+C_{p2}} \quad (9)$$

The compensation capacitor Cc will probably be mitigated until C_{total} is equal to the unit capacitor Cn and for that Reason, the L-side capacitance range has the right weight over the charge redistribution. The required capacitance of C_c is simply calculated as;

$$C_c = 31(C_B + C_{p2}) - 32Cn - C_{p1} \quad (10)$$

In this design, the C_B and C_c values are chosen as 32.5 fF and 2.5 fF respectively. Applying these exact capacitance estimations of both C_B and C_C, mismatches and parasitic capacitance effects to linearity malfunction implementation might be well controlled.

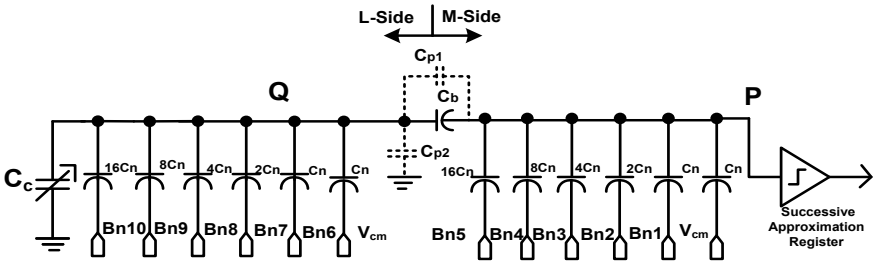

Figure 6. The Architecture of proposed DAC with calibration

2.5. SAR and its control logic

The SAR plays a key role in generating clock signals. These clock signals are connected to clk_i of DAC control logic [21]. The dynamic comparator outputs are connected to the NAND gate to generate valid signal. The sampling clock signal acts as a clock to the register. The schematic of SAR and control logic is displayed in Figure 7. and Figure 8. The output of the last flip-flop of this register, a valid signal from comparator, and sampling clock signals are connected to an OR gate, to produce the ClkC signal. This ClkC signal acts as a control to the dynamic latch comparator. The DAC control logic consists of a flipflop, AND gate, buffer, and inverter. The clocks from the successive approximation register act as sampling clocks to the control logic. These clocks sample the comparator output either (outp or outn) and produce output according to logic. In case the output signal of this comparator is high, then the outcome signal of the AND gate is high and will probably be attached as input into the inverter. If the AND gate output is at logic high, the ground voltage will appear as the output to the control logic. If the output of the AND gate is low, the reference voltage will appear at the output. The delay buffer is used to trigger the Clki signal at the input of the AND gate after flipflop.

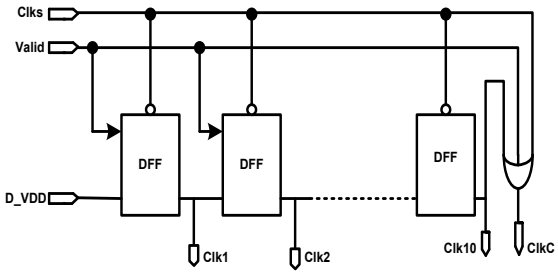

Figure 7. The schematic of SAR

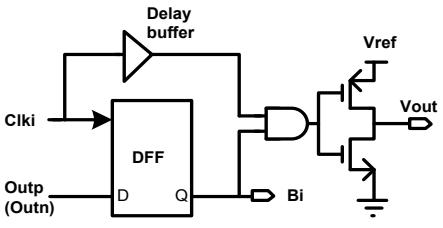

Figure 8. The schematic of control logic

3. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed bootstrap switch used in full differential structure gives improved linearity. Figure 9 shows the comparison of conventional bootstrap circuit with the proposed bootstrap. Nearly 35% of the linearity improvement is observed. The input range of the proposed SAR-ADC is 1.1 V peak to peak above the origin. Most of the wireless implantable system signals have a bandwidth between 10kHz to 15 kHz. Thus, the intermediate frequency 12.69 kHz has been chosen as an input frequency using a coherent sampling calculator

method. The sampling frequency is 200kS/s. From these input and sampling frequencies, one can say that this application follows Nyquist criteria. i.e $f_s >= 2f_m$. Figure 10. shows the 5120-point FFT spectrum. The quantified spurious free dynamic range (SFDR) will be 58.62 (dB). The signal to noise ratio (SNR) and the effective number of bits (ENOB) is 61.96 (dB) along with 9.41 (bits) respectively. Table-I enumerates the functioning parameters of the SAR ADC with other reference papers. Another performance parameter is figure of Merit [22, 23] and it can be characterized as;

$$\text{FoM} = \frac{\text{Power}}{2^{\text{ENOB}} * f_s} \tag{11}$$

In the above equation ENOB is the effective number of bits and f_s is the sampling frequency. As the sampling frequency increases the FoM decreases and power dissipation will be increased. Compared with reference [23-25] this ADC FoM achieves better results and the value is 3.15(fJ/conv-step) at 200kS/s sampling rate. This is due to the low power consumption of the proposed SAR-ADC. The power dissipation of single- ended SAR ADC is 3.277 µW. It is observed that the power consumption of the proposed work is 422.3 nW, which is very much less compared to the other works reported (Table 1). ence, this circuit is suitable for WIS.

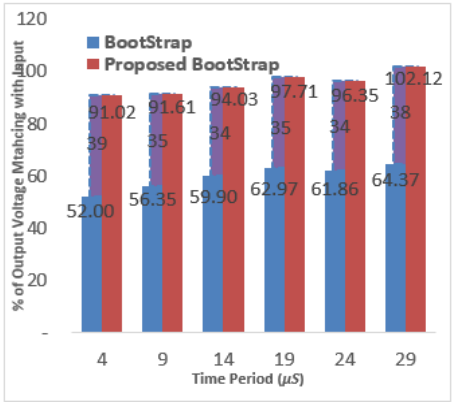

Figure 9. Comparison of linearity improvement of bootstrap and proposed bootstrap design

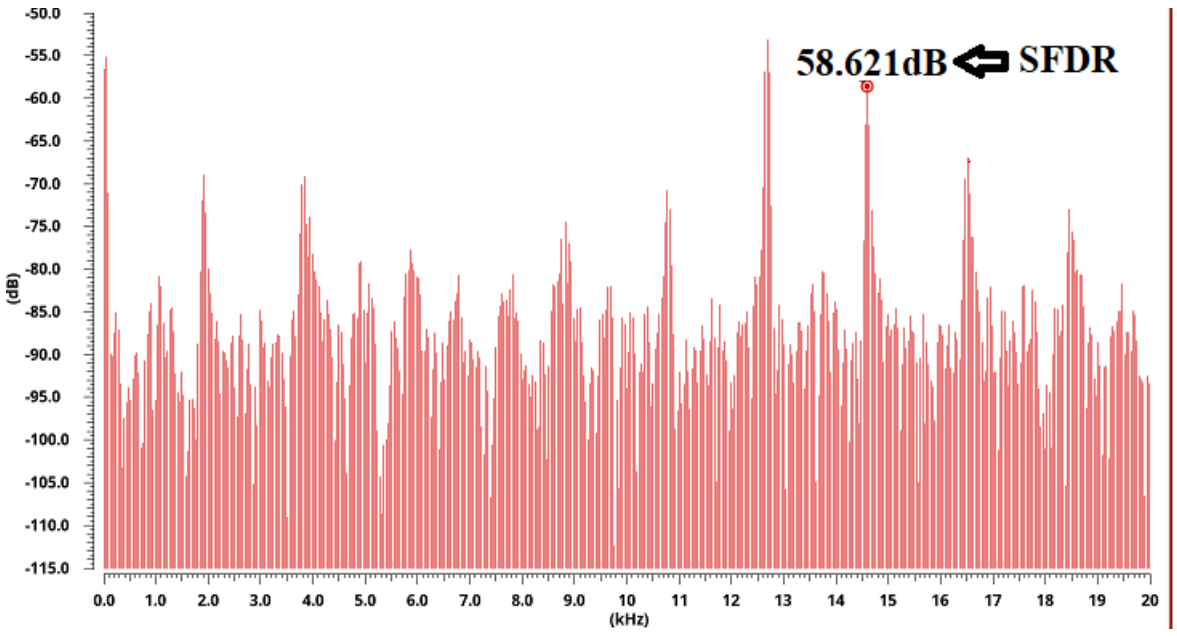

Figure 10. Power spectral density of SAR ADC

Table 1. Performance comparison of proposed SAR ADC with existing SAR ADCs

Parameter	TCAS.II 2016[23]	ASSC'2015[24]	MJ. ELSVIE.2016[25]	Proposed work
Technology(nm)	180	180	90	45
Resolution(bits)	10	10	8	10
Supply voltage(V)	0.8	1	1	1.1
Power (W)	200n	1.2µ	200n	422.3n
DNL/INL (LSB)	±0.5/0.1	±0.5/0.4	±0.4/0.92	±0.4/0.2
ENOB (bits)	9.05	9.48	7.6	9.38
FoM (fJ/conv-step)	1.88	24.1	11.1	3.15
SFDR (dB)	-	-	40.3	58.62

Nearly, 87.3% of power consumption is reduced with the usage of Split capacitance DAC with calibration. The ENoB obtained is 9.38 bits as against 10 bits. A considerable improvement is also observed in the values of SFDR. The comparison of power consumption at different sampling frequencies of conventional and proposed SAR ADC is shown in Figure 11. The bridge capacitance value is taken as 32.5 fF to reduce the DAC mismatch. The total capacitance of conventional SAR ADC is 512 C and the capacitance of proposed SAR ADC with Calibration is 47.5 C. The Spurious Free Distortion Ratio (SFDR) at 200kS/s is -58.62dB. The Figure 12 shows that nearly 4dB improvement at different Sampling frequencies. To improve the accuracy of the digital to analog converter the calibration capacitor can be trimmed in different technologies or can be applied to different calibration algorithms.

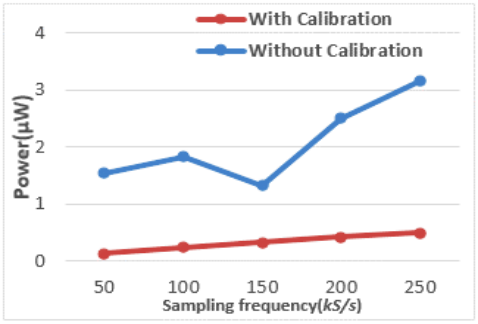

Figure 11. Comparison of power consumption with and without calibration of SAR-ADC

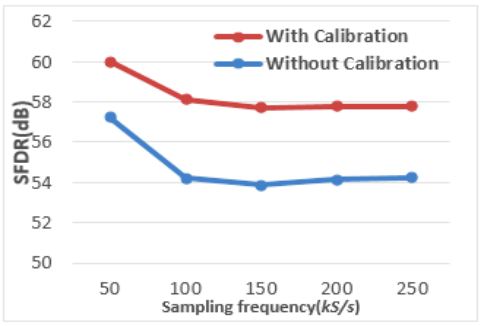

Figure 12. Comparison of SFDR at different Sampling frequencies with and without calibration

4. CONCLUSION

In this research paper, a high linear, low power, SAR-ADC for the wireless implantable system has been proposed. This SAR ADC is designed with a clock booster, the bootstrap circuit with a dummy switch, split capacitance DAC with calibration, dynamic latch comparator with reduced mismatch, and offset voltage. And the other blocks are successive approximation register and control logic. Low power is accomplished with all the usage of split capacitance DAC array. Nearly 87% of power consumption is reduced. The delay of the SAR ADC is 11.718µSec. High linearity is achieved with the usage of a clock booster, bootstrap with dummy switch in a full differential manner. Operating at 1.1V supply voltage and 200kS/s the proposed ADC attains SFDR of 58.62(dB), at 9.38 (bits) of an effective number of bits. This design achieves with the power consumption of less than 0.5 µW and FoM of 3.12fJ/conv-step.

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