TELKOMNIKA, Vol.12, No.2, June 2014, pp. 283~290
ISSN: 1693-6930, accredited A by DIKTI, Decree No: 58/DIKTI/Kep/2013
DOI: 10.12928/TELKOMNIKA.v12i2.1870

Bipolar-CMOS-DMOS Process-Based a Robust and High-Accuracy Low Drop-Out Regulator

Pan Luwei[1], Zhou Li*[1], Sun Tao[2]
[1] School of Information Science and Engineering, Shandong University,
No.27, South Shanda Road, Jinan 250100, China, Ph./Fax:+86-053188361623
[2] Shandong Provincial Key Laboratory of Network based Intelligent Computing, University of Jinan,
No.336, West Nanxinzhuang Road, Jinan 250022, China, Ph./Fax:+86-053182767503
* Corresponding Author, e-mail:zhou_li@sdu.edu.cn

Abstract

*A high-accuracy and robust Low Drop-Out Regulator was proposed and tape-out in CSMC 0.5um 40V BCD process; the LDO was integrated in a LED Control and Driver SOC of outdoor applications. The proposed LDO converted the 12V~40V input power to 5V for the low voltage circuits inside the SOC. The robustness of LDO was important because the application condition of the SOC was bad. It was simulated in all process corner, -55℃~150℃ temperature and 12V~40V power voltage conditions. Simulation result shows that the LDO works robustly in conditions mentioned above. The default precision of LDO output voltage is ±2.75% max in all conditions, moreover, by utilizing a trim circuit in the feedback network, the precision can be improved to ±0.5% max after being trimmed by 3 bit digital trim signal Trim[3:1]. The total size of the proposed LDO is 135um*450um and the maximum current consumption is 284uA.*

Keywords: *BCD process, LED Driver, Low Drop-Out Regulator, Digital trim signal*

1. Introduction

Nowdays, Light Emitting Diode (LED) lamps are widely used in decorative lighting because LED has many advantages. In contrast to traditional lighting sources, LED has lower energy consumption, longer lifetime, smaller size and improved physical robustness[1],[2]. In outdoor decorative lighting application, LED lamps are used outside the building to form pictures or videos. Because the outdoor environment vary significantly among seasons and places, the robustness of LED Drivers is important. A robust Low Drop-Out Regulator (LDO) is designed which is used in a Bipolar-CMOS-DMOS (BCD) process LED driver System on a Chip (SOC). The proposed LDO provides a 5V power for LED control circuit, serial transmitter and receiver in SOC.

BCD process Integrated Circuit (IC) has been widely used in the field of green energy-saving products especially LED drivers. It manufactures bipolar devices, CMOS devices and DMOS devices on the same chip. It combines the advantage of the high trans-conductance and strong load-drive capability of BJT device, high integration density and low power of CMOS devices and high power output of DMOS power devices[3],[4].

The LED driver SOC is designed to be used in harsh outdoor environment. The robustness of the LDO is guaranteed by a wide voltage and temperature range design. For different LED display applications, the input voltage of the SOC varies from 12V to 40V depending on the number of LED lamps needed to be driven. The working temperature range of the LDO is from -55℃ to 150℃. Meanwhile, the proposed LDO can drive 200mA current maximally. The specification of the proposed LDO is shown in Table1.

Table 1. Specification of LDO

Item	Specification		
	Min	Typical	Max
Reference Voltage Accuracy	-1.5%	0(1.21V)	+1.5%
Output Voltage Accuracy	-3%	0(5V)	3%
Line Regulation Rate	-2.5%	0	+2.5%
Load Regulation Rate	-2.5%	0	+2.5%
Quiescent Current		300uA	500uA
Load Drive Current		100mA	200mA

Received November 8, 2013; Revised March 18, 2014; Accepted April 2, 2014

2. Design and Analysis of LDO

As is shown in Figure1, the proposed high-accuracy and robust LDO includes Bandgap Reference (01), Error Amplifier (02), Feedback Network (03), Pass Element PMOS transistor P0 (04), and Frequency Compensation Capacitor Cc (05) [5]. VDDH is the input supply voltage; Bandgap Reference (01) generates a reference voltage VBGR which is around 1.21V; Error Amplifier (02), Feedback Network (03), Pass Element P0 (04) and Frequency Compensation Capacitor Cc (05) constitute the regulation loop of LDO; the output of LDO is VDDL which is a 5V stable voltage. The Error Amplifier (02) provides gain for the regulation loop. A 3 bit digital control signal Trim[3:1] controls the Feedback Network (03) to trim the LDO output voltage by changing the sampled feedback voltage VFB. When the output voltage deviates from the design specification caused by process variations, the output voltage can meet the requirements by adjusting Trim[3:1]. The Pass Element (04) drives large amounts of current. The phase margin of regulation loop is improved by the Frequency Compensation Capacitor Cc (05).

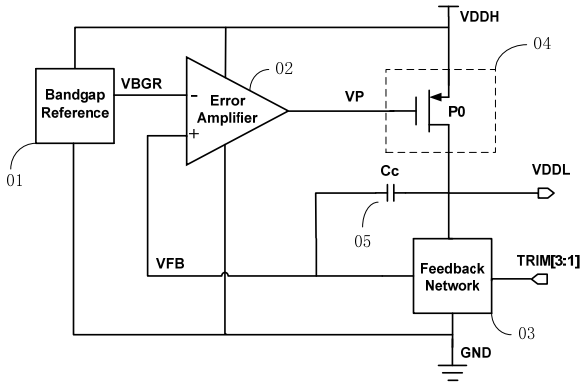

Figure1. Block diagram of the proposed LDO

Considering different application conditions, to make the LDO work robustly in all situations, the simulation case must cover all process corner, temperature and power voltage conditions. The LDO is simulated on all process corners including Typical-nmos-Typical-pmos case(TT), Fast-nmos-Fast-pmos case(FF), Slow-nmos-Slow-pmos case (SS), Fast-nmos- Slow pmos-case (FS) and Slow-nmos-Fast-pmos case (SF); 25□ room temperature, 150□ high temperature and -55□ low temperature; 24V normal voltage, 40V high voltage and 12V low voltage conditions. The robustness of LDO in 150□ high temperature condition is the most important point of the design.

2.1. Reference Voltage

The reference voltage produced by ideal reference voltage source should be stable when supply voltage, process and temperature vary.It provides the reference voltage (VFB) for LDO to produce output voltage. The precision and temperature characteristics of reference voltage determine that of the output of LDO. In actual design, Bandgap Reference circuit is the best choice for reference voltage source[6]. As is shown in Figure 2, the Bandgap Reference includes Startup Circuit (11), Proportional to Absolute Temperature (PTAT) Current Generation Circuit (12), Reference Voltage Generation Circuit (13). Startup Circuit (11) consists of resistor R15 and NMOS transistors N15, N16, it is used to prevent the reference voltage source in zero state during power on process. PTAT Current Generation Circuit (12) generates a positive temperature coefficient current, and PMOS P15 and P16 in the Reference Voltage Generation Circuit (13) mirror the PTAT current. It flows through the resistor R14 and transistor Q13 with a negative temperature coefficient to generate a 1.21V Bandgap Reference voltage (VBGR) [7]. Since the input supply voltage VDDH varies from 12V to 40V, 40V high voltage MOS transistors are used. High voltage NMOS transistors N11, N12, N13, N14 and high voltage PMOS transistors P11, P12, P13, P14 and resistors R11, R12, R13 constitute self-bias cascode circuit

to improve the Power Supply Rejection Ration (PSRR) of the Bandgap Reference[8]. The simulation results show that the Bandgap Reference circuit can provide 1.21V reference voltage in all process corner, -55□~150□ temperature and 12V~40V power voltage conditions. The temperature coefficient is 6.2ppm/□ @ typical case.

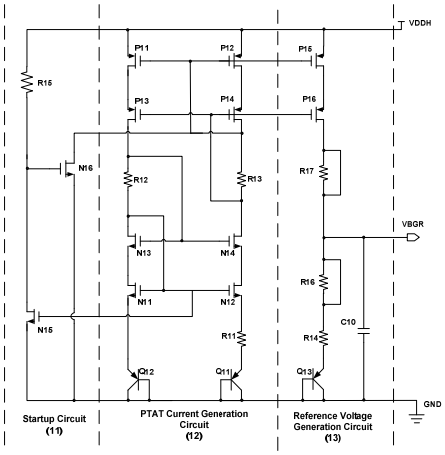

Figure 2.Bandgap Reference circuit

2.2. Error Amplifier and Pass Element

The regulation loop of the proposed LDO consists of Error Amplifier (02), Feedback Network (03), Pass Element (04) and Frequency Compensation Capacitor (05). The Error Amplifier (02) provides gain for the regulation loop; its performance has significant effects on the LDO[9]. Since the input supply voltage VDDH of LDO is 40V high voltage in contrast with the 5V ouput voltage VDDL, in order to make the LDO work robustly, especially when the load current is around several micro Ampere, the output VP of the Error Amplifier (02) should produce a voltage close to the supply voltage to make the Pass Element driving small load current. Thus, a class-AB stage is used as the output stage of Error Amplifier to generate large output voltage swing[10].

Figure 3 shows the circuit of Error Amplifier (02). The two inputs are connected to the output VBGR of Bandgap Reference (01) and the feedback voltage VFB from the Feedback Network (03) individually. Since the voltage VBGR is 1.21V and when the LDO works, the voltage of VFB is around 1.21V too. A pair of large-sized PMOS transistors P21 and P22 is used as the input of Error Amplifier (02) to ensure the transconductance and matching of the input stage.In the output drive stage of Error Amplifier (02), the size of MOS transistors N24 and P24 are set to four times that of N23 and P23 to ensure that the Error Amplifier has enough drive capability and voltage slew rate, higher bandwidth and voltage slew rate will improve the transient response of the LDO.

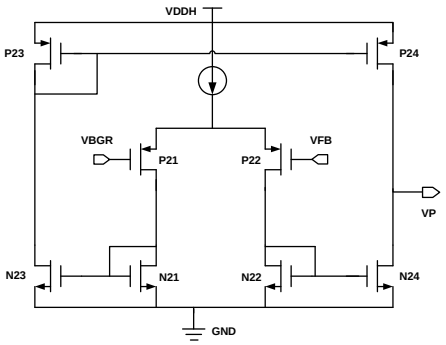

Figure 3. Error amplifier

The size of the Pass Element (04) must be large enough to drive large current. As shown in Figure 1, multi-finger structure and large size of high voltage PMOS transistor P0 are used to make the LDO provide 200mA load current accroding to the LDO's specification. However, the large Pass Element PMOS transistor has large capacitance which leads the second dominant pole move to the low-frequency and makes the phase margin of the regulation loop worse[11]. So it is necessary to improve the phase margin of regulation loop by the Frequency Compensation Capacitor (05).

2.3. Frequency Compensation

As shown in Figure 1, the Frequency Compensation Capacitor Cc (05) is connected between the output of LDO and the feedback end (VFB) of Feedback Network[12]. By adding the Frequency Compensation Capacitor (05), a pair of pole and zero is generated to play the role of frequency compensation. Figure 4 shows the small signal model of the LDO proposed in Figure 1. Roa is the output resistance of the amplifier, Ro_pass is the output resistance of the pass element, gma and gmp refer to the transconductance of the amplifier and the pass element, Cpar is the parasitic capacitance introduced by the pass element, Co and Resr are the capacitance and the electrical series resistance of the output capacitor, Cb is the bypass capacitor and RL is the load resistance.

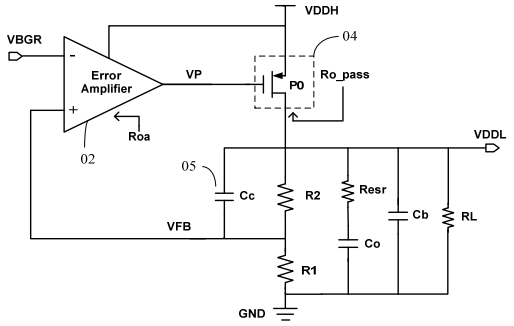

Figure 4. Small-signal model of LDO circuit

In Figure 4, disconnect the feedback loop at point VFB, the open-loop gain Av is:

$$A_V = g_{ma} R_{oa} \cdot \frac{g_{mp} Z}{1+SR_{oa}C_{par}} \cdot \frac{R_1(1+sC_cR_2)}{R_1+R_2+sC_xR_1R_2} \quad (1)$$

Where Z is the impedance seen at output VDDL, because the output capacitance is much larger than the bypass capacitance $C_o \gg C_b$:

$$Z = R_{o\_pass} // \left(R_{esr} + \frac{1}{sC_o}\right) // \frac{1}{sC_b} \approx \frac{R_{o\_pass}\,[1+sR_{esr}C_o]}{[1+s(R_{o\_pass}+R_{esr})C_o][1+s(R_{o\_pass}//R_{esr})C_b]} \quad (2)$$

By equation (1) and (2), we obtain that the transfer function of the LDO has the following four poles and two zeros:

$$P_1 \approx \frac{1}{2\pi R_{o\_pass}C_o} \quad (3)$$

$$P_2 \approx \frac{1}{2\pi R_{esr}C_b} \quad (4)$$

$$P_3 \approx \frac{1}{2\pi R_{oa}C_{par}} \quad (5)$$

$$P_c \approx \frac{1}{2\pi(R_1//R_2)C_o} \quad (6)$$

$$Z_1 \approx \frac{1}{2\pi R_{esr} C_o} \quad (7)$$

$$Z_c \approx \frac{1}{2\pi R_2 C_c} \quad (8)$$

Poles P1、P2、P3 and the zero Z1 belong to the regulation loop of LDO without Frequency Compensation Capacitor (05) [13]. Since the loop gain of LDO doesn't drop to 0dB at the frequency where the pole P3 resides, the phase margin of the loop is less than 45 ° which may cause the LDO unstable. In Figure 4, the effect of Compensation Capacitor Cc (05) is that a pole-zero pair Pc and Zc are added. The frequency of the zero Zc resides is close to the frequency of pole P3 resides, so the zero Zc will compensate the phase shift caused by pole P3. According to eqution (5), (6) and (8), the frequency of pole Pc resides is higher than pole P3 and zero Zc reside. Figure 5 shows the pole-zero location of the compensated loop, after P3 has been compesated by Zc, the loop gain of LDO drops to below 0dB at the frequency where the pole Pc resides, thus the phase margin of the regulation loop can achieve to more than 45 °and the stability of LDO is improved [14].

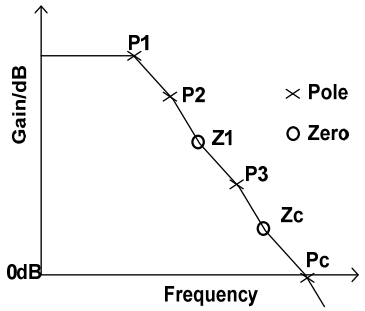

Figure 5. Pole-zero location

2.4. Feedback Network and Trim Control Circuit

The different application condition and tape-out process parameter variation will make the Bandgap Reference output VBGR deviate from the design specification which will make the voltage of LDO's output VDDL deviate from 5V. Therefore, the Feedback Network uses 3bit digital control signal Trim[3:1] to trim the output voltage VDDL. As shown in Figure 6, by setting different digital signal Trim[3:1] , the 8 to 1 Analog Switch can select different channel (CH1 ~ CH8) to change the feedback voltage VFB, the voltage of VDDL is also changed by it.

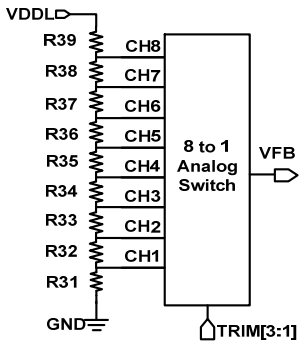

Figure 6. Resistor feedback network

The mapping relationship between the digital control signal Trim[3:1] and the LDO's output voltage VDDL is shown in Table 2.The minimum value of VDDL is 4.8V when Trim[3:1] is 000. The default voltage of VDDL is 5V when Trim[3:1] equals to100 and the maximum voltage of VDDL is 5.15V when Trim[3:1] equals to 111. As Trim[3:1] increases from 000 to 111, the voltage of VDDL increases 50mV per bit. After tape-out, if the process deviation makes the voltage of VDDL higher than 5V when Trim[3:1] equals to 100, Trim[3:1] can be set lower to make the voltage of VDDL smaller; if the process deviation makes the voltage of VDDL smaller than 5V when Trim[3:1] equalsto 100, Trim[3:1] can be set higher to make the voltage of VDDL higher.

Table 2. Mapping between Trim[3:1] and VDDL

Trim[3:1]	VDDL（V）
000	4.8
001	4.85
010	4.9
011	4.95
100(default)	5
101	5.05
110	5.1
111	5.15

2.5. Layout Design

As the proposed LDO involves high voltage device, the space and isolation between 40V high voltage devices and 5V low voltage devices are particularly important. Meanwhile, since the LDO drives a 200mA load current, place and route of Pass Element plays an important part in LDO's performance especially its efficiency. The layout design of the proposed LDO is based on CSMC 0.5μm 2P3M BCD process which supports 2 poly layers and 3 metal layers. The top metal is thick Aluminum and its current density is large. Parallel routing of Metal 2 and Metal 3 is used for routing of pass element to reduce the wiring resistance. The space between high voltage device and low voltage device should be large enough to reduce the cross interference. Figure 7 shows the layout of the Control and Driver SOC and the position of LDO in the SOC. LDO provides power for the LED signal receiver circuit and LED drive control circuit inside the SOC. The area size of the proposed LDO is 135um*450um.

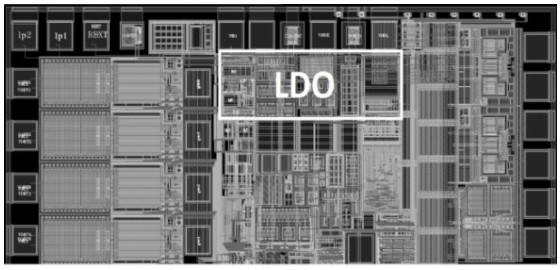

Figure 7. Layout of the LDO inside LED Drive and Control SOC

3. Simulation Results

The line regulation simulation results are show in Figure 8, set the load current of the LDO to 200mA and perform a transient simulation that when the LDO powers up, the supply voltage VDDH is 24V, make the supply voltage jump from 24V to 12V in 1us and from 12V to 24V in 1us, then the supply voltage jumps from 24V to 40V in 1us and from 40V to 24V in 1us (shown in the lower block of Figure 8). Corners, best case and worst case simulation waves of VDDL is shown in the upper block of Figure 8, the maximum deviation of VDDL when VDDH jumps is less than ±100mV, that is ≤ ±2% to the default value of VDDL.

The load regulation simulation results are show in Figure 9, set the supply power of the LDO to 12V, 24V and 40V individually, perform a transient simulation that when the LDO powers up, the load current jumps from 0mA to 200mA in 1us and from 200mA to 0mA in 1us (shown in the upper block of Figure 9). Corners, best case and worst case simulation waves of VDDL is shown in the lower block of Figure 9, the maximum deviation of VDDL when load current jumps is less than ±87.5mV, that is ≤ ±1.75% to the default value of VDDL.

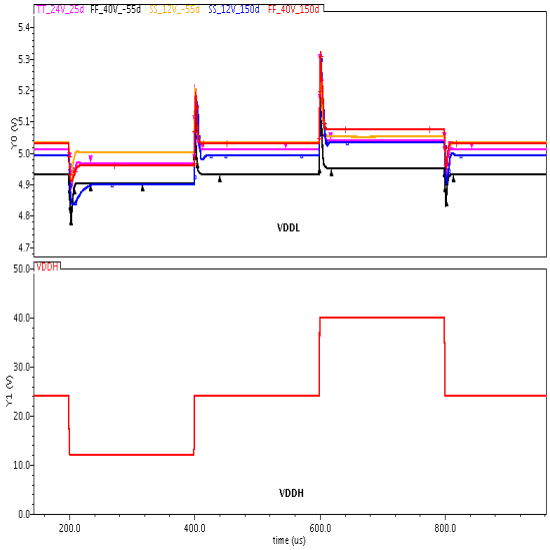

Figure 8. Simulation results of Line Regulation Character

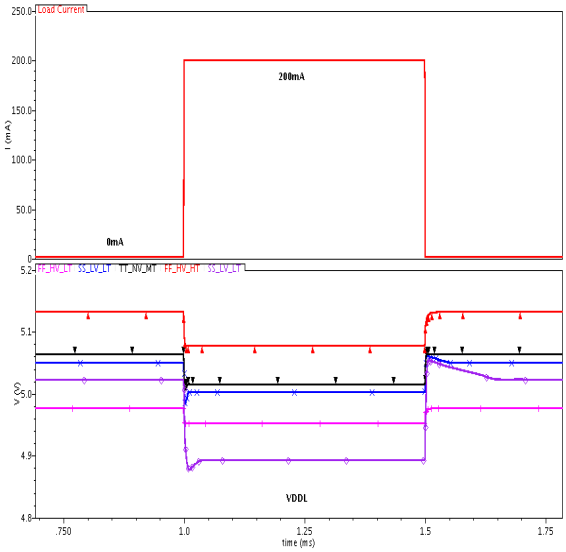

Figure 9. Simulation results of Load Regulation Character

The detailed simulation results are shown in Table 3. The simulation results show that the proposed LDO in this paper has good performance in all simulation cases including process corners, -55□~150□ temperature and 12V~40V power voltage conditions. The Output Voltage Accuracy is ±2.75% max by all simulation conditions before trim, thus we can eliminate the output voltage deviation caused by the tape-out process parameter variation through the digital control signal Trim[3:1]. As each step of the digital control signal Trim[3:1] can make the output voltage change 50mV and the Trim range is -4% to +3%, so the actual Output Voltage Accuracy can be improved to ±0.5% (25mV) max after being trimmed by Trim[3:1].

Table 3. Simulation Results

Simulation Items	Simulation Results
Load Drive Current	≥215mA
Quiescent Current	≤284uA
Load Regulation Rate	±1.75%
Line Regulation Rate	±2%
Loop Gain	≥43.9dB
Phase Margin	≥53.7º
Reference Voltage Accuracy	±1.5%
Output Voltage Accuracy	≤±2.75%
Output Trim Range	-4% to +3%
Output Voltage Accuracy After Trimmed	≤±0.5%
PSRR	≥51.7@1kHz ≥43.5@10kHz ≥35.6@100kHz

4. Conclusion

A robust and high accuracy Low Drop-Out Regulator based on 40V BCD process is proposed, it's used in an outdoor decorative lighting LED Control and Driver SOC. Since the environment of outdoor applications varys significantly, the robustness of LED Drivers is important. The input supply voltage is 12V~40V and the output voltage supplies 5V power for other modules inside the SOC. Moreover, the application condition and the tape-out process variation would make the LDO's output voltage deviate from the specification, 3bit digital control signal Trim[3:1] and a trim circuit were used to improve the accuracy of the LDO's output voltage. The load current of LDO is 100mA typically and 200mA maximally while the quiescent current of the LDO is less than 284uA. Simulation results show that the proposed LDO works robustly in all process corner, -55℃~150℃ temperature and 12V~40V power voltage conditions. The default precision of LDO output voltage is ±2.75% max in all conditions, moreover, the precision can be improved to ±0.5% after being trimmed by 3 bit digital control signal Trim [3:1].

References

[1] Nan C, Henry SHC. A Driving Technology for Retrofit LED Lamp for Fluorescent Lighting Fixtures With Electronic Ballasts. *IEEE TRANSACTIONS ON POWER ELECTRONICS.* 2011; 26(2): 588-589.
[2] Hongming Y, Jan WMB, Tim CWS. Illumination Sensing in LED Lighting Systems Based on Frequency-Division Multiplexing. *IEEE TRANSACTIONS ON SIGNAL PROCESSING.* 2009; 57(11): 4269-4270.
[3] Zhengyuan Z, Zhicheng F, Yong, Jiangen L, Xiaogang L. *A new method to reduce VDMOS on-resistance in BCD process.* 10th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT). Shanghai. 2010: 117-119.
[4] Chang-Tzu W, Ming-Dou K. ESD Protection Design With Lateral DMOS Transistor in 40-V BCD Technology. *IEEE TRANSACTIONS ON ELECTRON DEVICES.* 2010; 57(12): 3395-3396.
[5] Gabriel ARM, Phillip EA. A low-voltage, low quiescent current, low drop-out regulator. *IEEE Journal of Solid-State Circuits.* 1998; 33(1): 36-44.
[6] Bogoda A, Indika UK, Shunsuke O, Toru I, Kenji T. An Area-Efficient CMOS Bandgap Reference Utilizing a Switched-Current Technique. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.* 2010; 57(10): 762-763.
[7] Ming-Dou K, Jung-Sheng C. New Curvature-Compensation Technique for CMOS Bandgap Reference With Sub-1-V Operation. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS*. 2006; 53(8): 667-668.
[8] Behzad R. *Design of Analog CMOS Integrated Circuit*. ChenGuican, ChengJun, ZhangRuizhi. Xi' An: Xi' An Jiao Tong University Press. 2003: 324-325.
[9] Robert JM, Jose SM, Edgar SS. Full On-Chip CMOS Low-Dropout Voltage Regulator. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS.* 2007; 54(9): 1885-1886.
[10] Gianluca G, Gaetano P, Ester S. *Low-voltage LDO Compensation Strategy based on Current Amplifiers.* IEEE International Symposium on Circuits and Systems. Seattle, WA. 2008: 2681-2684.
[11] Tsz YM, Philip KTM, Mansun C. A High Slew-Rate Push–Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement. *IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS.* 2007; 54(9): 755-759.
[12] Xuewen W, Fengge W, Zhongwei L.*The Analysis of LDO and the Stability of Loop Compensation.* 2010 International Conference on Electrical and Control Engineering. Wuhan. 2010: 4368-4370.
[13] Gabriel ARM, Phillip EA. Optimized Frequency-Shaping Circuit Topologies for LDO's. *IEEE Transactions on Circuits and Systems II Analog and Digital Signal Processing.* 1998; 45(6): 703–708.
[14] Phillip EA, Douglas RH. *CMOS Analog IC Design*. FengJun, LiZhiqun. Beijing: Electronic Industry Press. 2011: 206-207.